MITIGATION OF HARMONICS IN VARIABLE FREQUENCY DRIVE USING MULTILEVEL INVERTER

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Abstract— This method is proposed with pulse width modulation (PWM) rectifier. It can be used to regulate the input power quality of variable frequency drives (VFDs). The PWM rectifier is an AC to DC power converter. The electro-mechanical drive systems are using VFDs to control AC motor speed and torque by varying motor input frequency and voltage. While passive filtering and current injection networks are the current techniques but it suffer from bulkiness, complexity, and performance issues at light loads. PWM technique provides less load-dependent performance. This paper introduces a study of improving the input power quality of a single phase to three phase rectifier-inverter structured VFD by using bridgeless dual boost(BLDB) PWM converter. .

***Keywords*—Variable frequency drive, bridgeless dual boost PWM converter, multilevel inverter, pulse width modulation, power quality**

I. INTRODUCTION

VFDs are largely used in the industry. It is adjustable speed drive used in electromechanical drive systems to control motor speed and torque by varying motor input frequency and voltage. It provide precise control over the torque and speed of the motor. It is nonlinear and inject a lot of harmonics into the grid resulting in poor power factor (PF), and total harmonic distortion (THD). Typically, a full bridge rectifier is maintained, where diode will only conduct when the instantaneous value of the line voltage gets higher than the average value of the DC-link voltage. As a result, power is delivered through the rectifier as high amplitude pulses leading to component stress, increased client bills, and limitation of the grid capacity. Several studies have been introduced in the literature to manipulate the problem of poor input power quality of VFDs.

One of the applied solutions is passive filtering technique using large line side reactors to reject high frequency harmonics, yet they are bulky and relatively expensive. Moreover, the source impedance highly impacts the performance of line reactors. Another approach is the active filtering through active front end (AFE) AC-DC converters which can be

thyristor based that achieves PFC of the drives by adjusting the motor flux in a narrow range to vary the DC-link current and hence regulating the input PF. However, this method results in a remarkable DC link current ripple, and it is restricted to the limited range of flux adjustment so as not to affect motor performance. A different solution applies the technology of selective harmonic elimination (SHE)/ selective harmonic compensation (SHC). Basically, a Fourier analysis is performed to the input current waveform.

The dominant harmonics are determined (usually 5th, 7th, and 11th harmonics), and a current injection circuit (can be star-delta transformer, zigzag transformer, or an LC tuned filter) is designed accordingly to compensate for the targeted harmonic components. While this method is convenient at high power applications, it is influenced by the design of the current injection network. It also suffers from steep deterioration as load decreases . This study adopts the approach of line current shaping by PWM BLDB converter Fig.1. The selection of proposed topology is based on a detailed comparative study implemented in from the efficiency and performance point of view. This study reviews the BLDB PFC converter topology as one method among several means of power quality improvement which let us have a closer look at its performance under an AC input and a nonlinear load at the output like motor drive compared to the methods included at the reference studies, and proposes a solution to reduce the remarkably large capacitor at the DC-link. Since VFD systems include two stages of power processing, AC-DC rectifier followed by the drive inverter, the efficiency has a higher priority over cost. A brief comparison is performed indicating the merits of the BLDB topology over the normal boost converter with bridge rectifier. Design and simulation results are then provided using PSIM simulation software.

II. OBJECTIVE

A. PWM Rectifier Principle of Operation

When it comes to PWM rectifiers operating in continuous conduction mode (CCM), the following equation is applicable for a boost converter

$$d(t) = 1-(vg(t)/v)$$

The sinusoidal component of the duty cycle enables the emulated resistance (input impedance of the converter which is dependent of the duty cycle) to vary in a sinusoidal manner. As a result the

controlled inductor current tracks the line voltage waveform and hence PFC is realized.

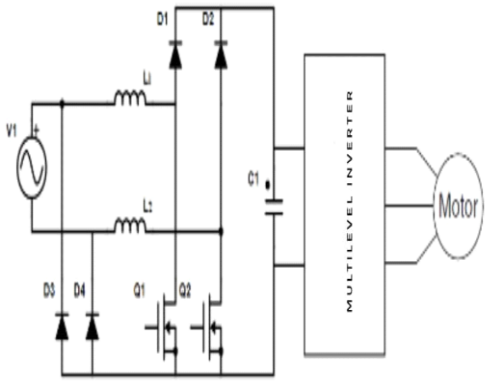

Fig. 1 Proposed PFC Converter Tropology

B. .BLDC Converter Design

The brushless dual boost converter consist of two branches. The two branches are operating alternatively. They are operating one by each half cycle. By using this configuration, it eliminates the need of bridge rectifier in this the line voltage of the system is rectified. The rectification can be done by the fast diode of the converter with a feedback diode. The use of fast diode and feedback diode leading to reduced losses over normal tropology. Fig 2 illustrated positive half cycle and fig 3 illustrate negative half cycle.

The comparison relied on Infineon semiconductors to calculate the converters losses. According to the IDP30E60 diode, its contribution to the power loss is 13.636W (-0.68%) at full load of 2kW and input voltage of 220Vrms. Since one rectifying diode is eliminated, the converter efficiency is increased in proportion to the power loss contribution of that diode. It worth pointing out that diode power loss is calculated according to while the reverse recovery loss is negligible. So the relation of diode loss to energy improvement percentage is linear and hence the +0.68% improvement is constant regardless of load percentage. Moreover, diodes D3 and D4 provide a feedback path to the line current. Otherwise, the line voltage would be floating with reference to the converter ground causing the line voltage sensor circuitry to be complex and requiring line frequency isolating transformer.

- Positive half cycle

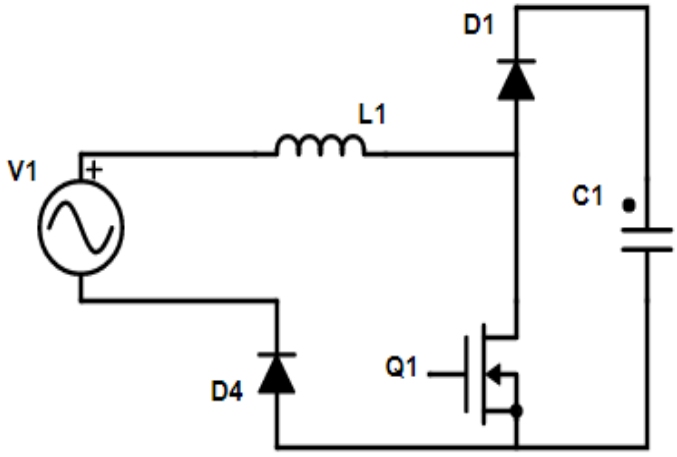

Fig. 2 Positive half cycle

- Negative Half Cycle

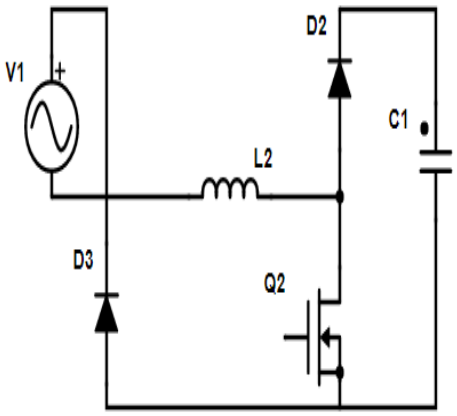

Fig.3 Negative Half Cycle

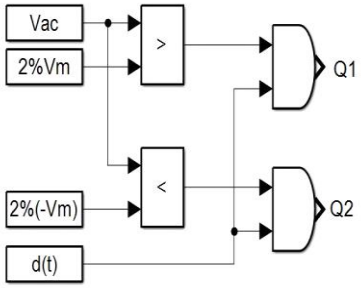

Fig. 4 Zero Crossing Circuit Applying Dead Period

The output duty ratio d(t) of the control system of Fig.4 is fed to an AND logical circuit along with the output of a zero crossing circuitry that detects the starting of each half cycle and operates the corresponding BLDB branch accordingly.

C. DC-LINK Capacitance Reduction

The power flowing through the DC link is constant. The instantaneous power delivered at the grid side is vary periodically. Due to this when the input power drops to zero the DC link voltage contain and AC oscillating component and the charge imbalance has to be compensated. the purpose of designing DC link capacitance is, it hold and provide a constant DC link average voltage for a full line cycle rather than a switching cycle of a PWM converter.

To reduce the DC link capacitance is to allow for a relatively large AC oscillating component and adjusting the motor drive control to compensate for the DC link oscillations. The minimum value of DC link voltage should atleast provide the maximum requirement of the motor is to be notice. Otherwise the drive will not be able to provide sufficient voltage to the motor due to the step down feature.

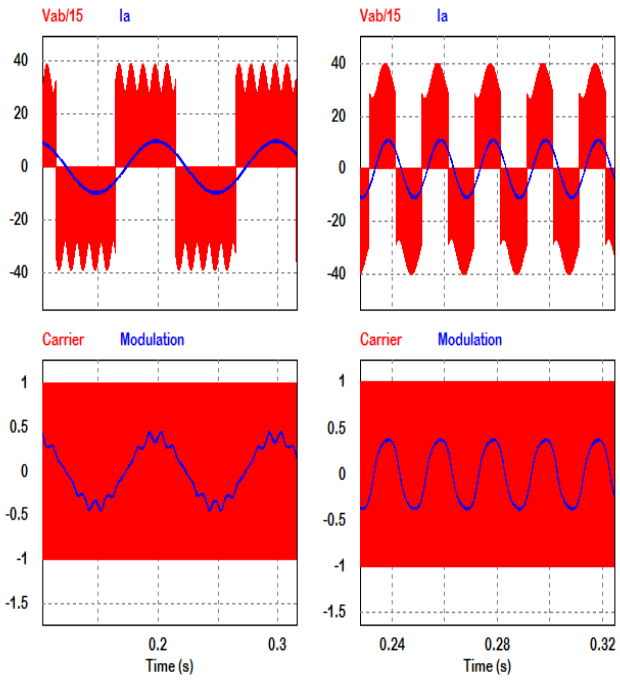

Fig. 5 Drive output and modulation signal

Above figure which indicate the drive able to compensate for the DC-link voltage modulation signal which is operating at 10Hz and oscillations and maintain proper output 50Hz. It increases at the instant where DC link voltage and hence sinusoidal motor voltage decreases and vice versa. current.

D. Control System Design

The PFC is power factor correction or power factor controller it is used to increasing power factor by using active electronic circuits with feedback that control the shape of the drawn current. It is used to shape the input current. There are many commercial PFC controller that can complete this task. A variety of control techniques is used to control the shape of input current but they are not successful. The average current mode control strategy is used. It provide sufficient immunity against noise hence it result to line voltage

Simulation Result and Discussion

The converter operates in the range of 90V/240V, 50/60 Hz. it exhibits better PF and THD at low voltage ranges for the same amount of load power. This is because of the low ratio of the current ripple component to the fundamental. On the other hand, PF declines and THD increases at light load where the ripple component dominates. This problem can be mitigated by selecting larger inductor without affecting the converter controllability. The drive controller was

At higher loads, the modulation index is larger to provide higher output current which is why the compensation effect is more obvious on the modulation signal of the Fig.9 at full load than at half load.

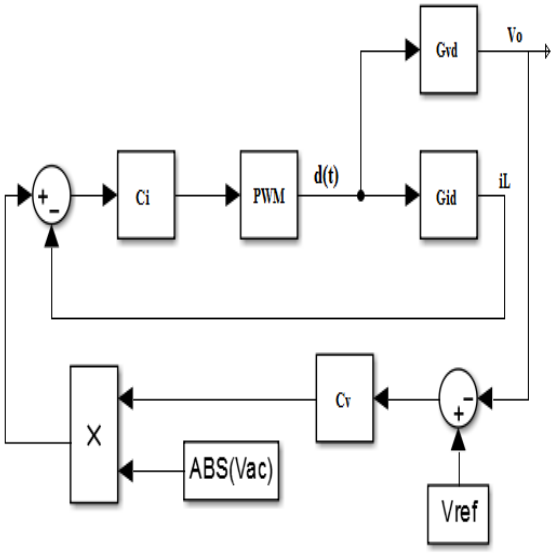

Fig.6 Control Algorithm of the PFC Converter.

It shows a PFC converter. It provide inner current control loop with 15.9KHz band width which is fed from a current sensor located at the ground path between switch Q1 and Diode D4.

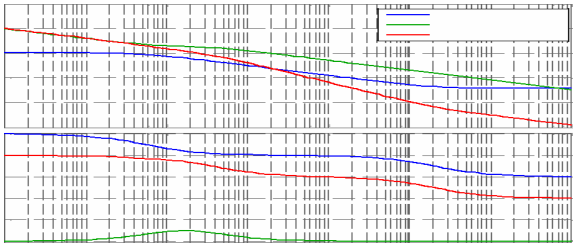

Fig 7. Voltage control loop characteristics

It was intentionally set slower to avoid distorting the current reference signal.

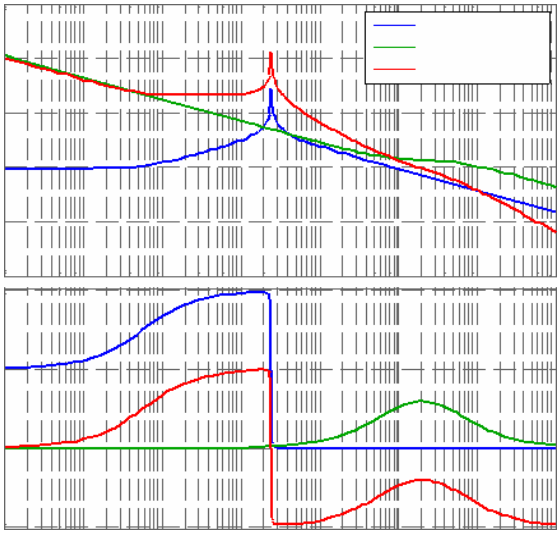

Fig 8. Current Control loop Characteristics

It is observed that a proportional integral controller is adequate to stabilize the current loop

III. CONCLUSION

A PWM BLDB converter is designed to regulate the input power of VFDs. This topology exploits the fast diodes of the boost converter to rectify the line voltage with the help of feedback diodes, hence it increasing efficiency over the existing topology. It provide superior performance. Can used for a wide range of loading conditions. The remarkable drawback is PWM converter operating as PFC is the output capacitance allowing for higher oscillations and compensating it through the drive controller without transferring those oscillations to the motor side.

IV. References

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