Analytical Modeling and Simulation of TFET

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***ABSTRACT*—In this paper, analytical model of Double Material TFET is presented. Expressions are derived for surface potential, electric field and the drain current is derived. Surface potential is derived by using 2D poisson equation. Parabolic approximation technique is used to solve 2-D poisson equation with the help of suitable boundary conditions. Expression for field along the channel length is obtained by differentiating the potential. Expression for drain current is obtained by integrating the tunnelling generation rate. Kane's method is employed to calculate tunnelling generation rate. Results are obtained by simulating it in MATLAB.**

***Index Terms*—Tunnel FET, parabolic approximation technique, poisson equation, surface potential, electric field, drain current.**

1. INTRODUCTION

The main challenge in scaling the CMOS device is to ensure about the better performance of the device and to improve its functionality. Several structures are available for maintaining the device characteristics. [1] Main disadvantage that limits CMOS device is increased short channel effects and very high leakage current. There are some devices which have been proposed to overcome SCEs but in these effects supply voltage cannot be reduced because of its limited subthreshold swing. [2] TFET is one of the promising candidate for future generation low power very large scale integration applications due to their very low subthreshold swing (even below minimum 60mv/decade) and low OFF current. [3], In TFET, electrons tunnel from source valence band to channel conduction band and this BTBT process is essentially responsible for current transport in these devices.

Major disadvantage of TFET is low ON-current as well as I_{OFF} may increase due to ambipolar behaviour because of leakage and this cannot be eliminated completely. I_{ON} is very low because of poor BTBT. Several techniques are available to improve the ON – current of TFET. Among them, using DM TFET structure enhances I_{ON} during device operation. In this method; surface potential, electric field distribution and drain current is calculated. It is also noted that the electrical characteristics of TFET can be improved by using stacked gate oxide of Sio_2 and high- k material in DM TFET instead conventional Sio_2.

The derivations for surface potential, electric field and drain current is derived in next section.

2. DERIVATION

Cross section view of DM TFET is shown in figure(1). Source is highly doped with p-type and drain is highly doped with n-type. Silicon dielectric is considered as the gate dielectric. Gate is made up of 2 materials G_1 and G_2 whose length is P_1 and P_2 with two different work function Ø1 and Ø2. If positive voltage is applied to gate then the transistor behaves as a n-TFET and when negative voltage is applied to gate, then the transistor behaves as a p-TFET. If positive voltage on gate is increased then the barrier between source and intrinsic region is decreased. Then the electrons move from valence band to the conduction band.

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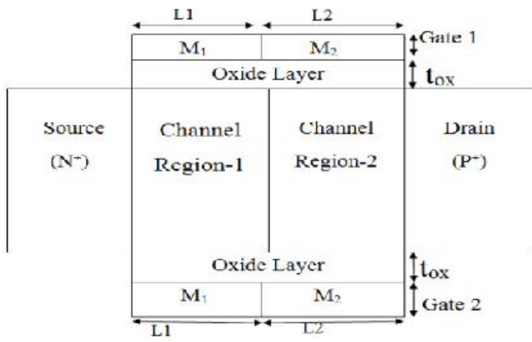

Fig 1: Structure of Double Material TFET

2.1 SURFACE POTENTIAL

Surface potential is found by 2-D poisson equation. Parabolic approximation technique is used to solve the poisson equation,

$$\frac{\partial 6^2(x,y)}{\partial x^2}+\frac{\partial 6^2(x,y)}{\partial y^2}=0 \qquad (1)$$

Surface potential along the vertical direction is given by

$$\theta(x,y) = a_0(x)+a_1(x)y+a_2(x)y^2 \qquad (2)$$

3 boundary conditions are considered along the channel length region.

i) Flux at front end:

$$\frac{d\ \ 1(x,y)}{d} = \frac{\epsilon o}{\epsilon s}\ \frac{\theta\ \ 1(x)-\sigma\ \ 1}{t_i}$$, at y=0 for G_1

$$\frac{d\ \ 2(x,y)}{d} = \frac{\epsilon o}{\epsilon s}\ \frac{\theta\ \ 2(x)-\sigma\ \ 2}{t_i}$$, at y=0 for G_2

ii) Flux at back end

$$\frac{d\ \ 1(x,y)}{d} = 0$$, at $y=t_{si}$ for G_1

$$\frac{d\ \ 2(x,y)}{d} = 0$$, at $y=t_{si}$ for G_2

iii) Potential at source and drain end

$\theta_1(x,y) = \theta_{S1}(0) = V_{BI}$

$\theta_1(P1+P2,0) = \theta_{S1}(P1+P2) = V_{BI}+V_{DS}$

Where V_{BI} = built in potential

E_g = band gap energy

q= charge

V_{GS}= gate to source voltage

V_{DS}= drain to source voltage

ε_{si} = relative permittivity of silicon

ε_{ox} = relative permittivity of oxide

iv) Potential under materials G_1 is

$\theta_1(x,y)= \theta_{s1}(x)+a(x)y+b(x)y^2$, $0<x<L_1$

Potential under material G_2 is

$\theta_2(x,y)= \theta_{s2}(x)+c(x)y+d(x)y^2$, $L_1<x<L_1+L_2$

Where a(x), b(x), c(x), d(x) are constants and are derived from boundary conditions i and ii

$$a(x) = \frac{\epsilon o}{\epsilon s\ \ t_i}\theta_{s1}(x) - \sigma_{g1}$$

$$b(x) = -\frac{1}{2}\frac{\epsilon o}{\epsilon s\ \ t_i}\theta_{s1}(x) - \sigma_{g2}$$

$$c(x) = \frac{\epsilon o}{\epsilon s\ \ t_i}\theta_{s2}(x) - \sigma_{g2}$$

$$d(x) = -\frac{1}{2}\frac{\epsilon o}{\epsilon s\ \ t_i}\theta_{s2}(x) - \sigma_{g2}$$

potential $\theta_{s1}(x)$ and $\theta_{s2}(x)$ under G_1 and G_2 is obtained from (iii) and (iv)

$$\theta\ \ 1(x) = a11e^{\lambda x} + a12e^{-\lambda x} + \sigma\ \ 1$$

$$\theta\ \ 2(x) = a21e^{\lambda x} + a22e^{-\lambda x} + \sigma\ \ 1$$

$$= \frac{\sqrt{2\epsilon o}}{\sqrt{\epsilon s\ \ t_i\ \ \ t_i}}$$

$$\sigma\ \ 1 = V \quad -\theta\ \ 1 + k + \frac{E}{2}$$

$$\sigma\ \ 2 = V \quad -\theta\ \ 2 + k + \frac{E}{2}$$

Where θ_1= 4.6ev

θ_2= 4.2ev

$$A_{11} = \frac{V1e^{-\frac{\lambda L}{2}} - V2 - \frac{\beta 1}{\lambda^2}}{e^{-\frac{\lambda L}{2}} - e^{\ \frac{\lambda L}{2}}}\ [1 - e^{-\frac{\lambda L}{2}}]$$

$$A_{12} = \frac{V1e^{-\frac{\lambda L}{2}} - V2 - \frac{\beta 1}{\lambda^2}}{e^{\ \frac{\lambda L}{2}} - e^{-\frac{\lambda L}{2}}}\ [1 - e^{-\frac{\lambda L}{2}}]$$

$$A_{21} = \frac{V2e^{-\frac{\lambda L}{2}} - V3 - \frac{\beta 2}{\lambda^2}}{1 - e^{\ \frac{\lambda L}{2}}}\ [1 - e^{-\frac{\lambda L}{2}}]$$

$$A_{22} = \frac{V2e^{\ \frac{\lambda L}{2}} - V2 - \frac{\beta 2}{\lambda^2}}{1 - e^{-\frac{\lambda L}{2}}}\ [1 - e^{-\frac{\lambda L}{2}}]$$

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2.2. ELECTRIC FIELD

Electric field distribution is found by differentiating the potential

$E_1 = \frac{d \quad 1(X)}{d} = A_{11}e^{\lambda x} - A_{12}e^{-\lambda x}$

$/E_2 = \frac{d \quad 1(X)}{d} = A_{21}e^{\lambda x} - A_{22}e^{-\lambda x}$

2.3. DRAIN CURRENT

Drain current is found by tunnelling generation rate (G). G can be calculated by using Kane's method.

$I_{DS} = \iint G\mathrm{d}x\mathrm{d}y$

$G(E) = A \frac{|E|^2}{\sqrt{E_g}} e^{(-B \frac{E_g^{3/2}}{|E|})}$

3. RESULT & DISCUSSION

SYMBOL	PARAMETER	VALUE
P	Channel length	30nm
P_1	Tunnelling gate length	10nm
P_2	Auxillary gate length	20nm
t_{ox}	Thickness of oxide layer	2nm
t_{si}	Thickness of silicon layer	10nm
$G_1 = \emptyset 1$	Work function of tunnel gate	4.6ev
$G_2 = \emptyset 2$	Work function of auxiliary gate	4.2ev

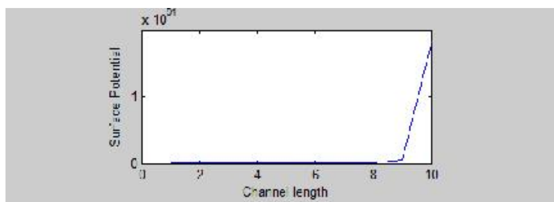

Fig 2: Channel length Vs Surface potential

The surface potential profile as a perform of position on the channel from the supply side to the drain side for DMDG TFET are obtained from modelled expression and MATLAB simulation. It is ascertained that as radius R decreases, the minimum value of surface potential decreases, and shifted towards the supply side, therefore indicating higher BTBT and decrease of V_{th} roll-off. Thus, it should be terminated that a reduction in channel radius causes in decrease of SCEs.

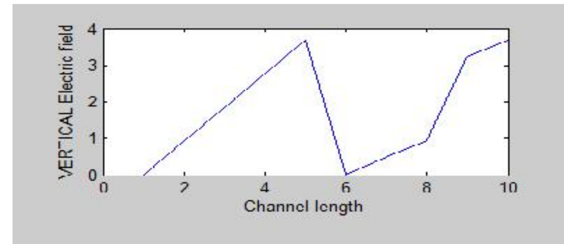

Fig 3: Channel length Vs Vertical electric field

The variation of the lateral electric field for DMDG TFET as a performance of the position on the channel from the supply side to the drain side with the results obtained from modelled expression and numerical MATLAB simulation. The rise within the electric field close to the junction of the dual-metals ends up in an increase within the carrier transport potency.

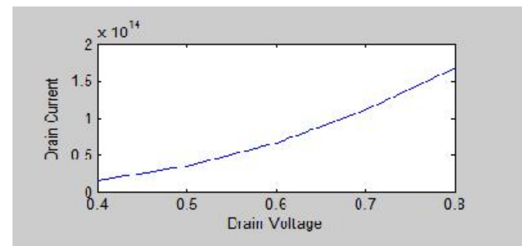

Fig 4: Drain Voltage Vs Drain Current

A high electric field close to the drain side could result in the formation of extremely energetic and accelerated "hot – carrier", that below the influence of transverse field could tunnel into the oxide, gets cornered into the oxide region and injury the interface. The reduction within the drain side electric field indicates a discount a reduction injurious Hot – Carrier Effects (HCEs).

The variation of subthreshold Drain Current (I_{DS}) as a performance of the V_{GS} for DMDG TFET is obtained

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from modelled expression and numerical MATLAB simulation. Rise in subthreshold drain current causes an increase in the subthreshold leakage current and decrease within the subthreshold swing that must be decreased for low power device applications.

4. CONCLUSION

In this DM TFET structure is analysed and their performance is discussed. This is based on fact that the surface potential is calculated by solving the poisson equation. Electric field distribution along the channel length is found by differentiating the potential. Drain current is based on band-to-band tunnel generation rate (G) and the current is found by integrating G. It is clear that by decreasing channel length DM TFET structure SCE is decreased.

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