A Survey on Binary Counter for Low Power Application

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***Abstract*—Binary counting of inputs is the necessary process in many applications such as reduction of partial products in multiplication. Counters are used to determine the number of ones for the multiple input logic. Thus, counters are most important and necessary to determine the active inputs in a multiple input logic. Hence counters determine the speed of the application such as multiplication. Hence the counter area must be reduced and speed of the counter is to be increased. In this paper the symmetric stacking binary counter is proposed such that the speed of the counter is increased than the conventional. Many Counters such as 2:2, 3:2, 4:3, 5:3, 6:3 and 7:3 counters are proposed in this paper.**

***Index Terms*—Binary Counters, Stacking Counters, Threshold Counters.**

1. INTRODUCTION

Parallel Counters are used in many designs and consequently have had many different implementations. These implementations use various basic building blocks such as (3,2) counters, (7,3) Counters. An (n,k) parallel counter is defined as having n input bits and producing a k-bit binary count of its "1" inputs, with $2^k - 1 > n$ or $k > [\log_2 (n+1)]$. A counter provides an exact count of its input that are 1 only if this is count is below a certain threshold. When the number of inputs that are 1 is either equal or exceeds the threshold, the output indicates only that the threshold has been reached and does not supply the exact count. Counters are useful in the design of the self-test and repair circuit for large memories embedded on a system on chip. Such a circuit counts the number of faulty bits. Further different type of counter techniques is discussed in this paper and their speed, area is discussed.

2. LITERATURE SURVEY AND ANALYSIS

Earl E. Swartzlander, JR. [1] proposed three separate types of counters. The first counter consists of a network of Full adders. The second counter uses the combination of Full adders and Fast adders (that may be realized with READ-ONLY memories), while the third type of counter uses quasi digital (ie analog current summing) techniques to generate an analog signal proportional to the count which is then digitized. The delay and complexity of each of the three counters is derived and compared. The full adder counter is slower than the fast adder counter, while the quasi digital counter appears to be proportionally faster than either of the strictly digital counters although it is more complex and it is prone to problems due to drift.

Hideaki Kobayashi and Hiroyoshi Ohara [2] proposed a method of parallel counting which enables small parallel counters to generate larger ones. It is an extension of the method of Carry Showers. A (u,v) counter is a small parallel counter with u inputs and v outputs, $u=2^V-1$. It is shown that the counter delay is proportional to the log of the number N of inputs and the total number of elements is approximated by N/(u-v). This counter is used to handle large number of inputs. Any scale of counters can be used as elementary blocks for the practical implementation of (u,v) counters the quasi digital appears to be potentially faster than the strictly digital ones.

Robert F. Jones et al.., [3] proposed a parallel counter implementation. An (n,m) parallel counter with n inputs that produces an m-bit binary count of the number of its inputs that are ones. This paper reports on the design of large parallel counters with up to 1022 inputs. Design trade-offs are examined regarding the use of counter cells of size ranging from (3,2) to (31,5) as building blocks. Here small, medium and large size counters are implemented and compared. In terms of both delay and area, the implementation which uses only (3,2) counters appears superior across the range of counter cell types.

Behrooz Parhami et al.., [4] proposed Accumulative Parallel Counters which represents a true generalization of a sequential counter in that it incorporates the memory feature of an ordinary counter. It adds the sum of its n binary inputs to a stored value. In this paper the design of accumulative parallel counter is examined and show that direct synthesis of such counter, as opposed to building it from a parallel counter and a fast adder leads to significant reduction in complexity and delay. It is useful in examining the large scale (systolic) associative processors. Modular multi operand adders, serial parallel multipliers and digital neural networks.

Shen-Fu Hsiao et al.., [5] This paper presents a 3-2 counter and 4-2 compressors which are the basic components in the partial product summation tree of a parallel array multiplier. A 3-2 counter using a full adder which is realized using an XOR/XNOR gate and two 2:1 multiplexer. The XOR/XNOR gate is realized using the Double pass transistor logic (DPL) circuit technique. The advantage of DPL is that both the inverting and non-inverting outputs are generated in the DPL implementation of logic gates. In this paper 4-2 compressors are presented by cascading the two 3-2 counters. In this case, the critical path of the compressor contains four cascaded XOR gates. For the improved implementation 4-2 counters are realized using six DPL MUXs. The analysis says that the DPL based 3-2 counter and 4-2 compressor are designed where the internal node capacitance on the critical path is reduced. It is also used to construct the partial product summation tree in the parallel array multiplier, significant improvement can be achieved in both delay and power performance.

D. Radhakrishnan [6] proposed Low Voltage Low Power Full Adder which can applied in the full adder counters and hence the speed of the counters is increased. These types of Full adders are designed with Pass transistor and Transmission gate logic. The formal design procedure for realizing a minimal transistor CMOS pass network XOR-XNOR cell, that is fully compensated for threshold voltage drop in MOS transistors is presented in this paper. This new cell can reliably operate within certain bounds when the power supply voltage is scaled down, as long as due consideration is given to the sizing of MOS transistors during the initial design step. A low transistor counts full adder cell using the new XOR-XNOR cell is presented. The speed and power calculations are determined in this paper. This new cell can be adopted for low voltage operation.

Zhoujun Wo et al.., [7] presented the saturating counters. Saturating counters are newly defined class of generalized parallel counters that provide the exact number of inputs which are equal to one only if this number is below a given threshold. Such counters are useful in self-test and repair units for embedded memories. This paper defines saturating counters for arbitrary threshold values and presents several alternatives for their implementation. The delay and area of the proposed counter are examined. In this the behavior of the saturated counters are studied. In the proposed saturating counter, the delay is reduced but the area overhead is increased.

Sreehari Veeramachaneni et al., [8] proposed the (m,n) parallel counters. Parallel counters are key elements in many arithmetic circuits such as fast multipliers. In this paper the architectures and design for high speed, low power (3,2), (7,3), (15,4) and (31,5) counters are capable of operating at ultra-low power voltages are presented. Based on these counters, a generalized architecture is derived for large (m,n) parallel counters. The proposed architecture lays emphasis on the use of multiplexers and a combination of CMOS and transmission gate logic in arithmetic circuits that result in high speed and efficient design. In this paper there is an improvement in the reduction of delay and power consumption.

Kirthi Krishna M et al.., [9] proposed an improvement in the above specified counters [8]. The proposed 3-2, 4-2 and 5-2 counters achieve better performance when compared with the existing counters. The power consumption and delay are compared with the existing counters. In the proposed architecture these outputs are efficiently utilized to improve the performance of the compressors. The combination of low power, low transistor count and lesser delay makes the new compressors viable option for efficient design.

Mahnoush Ruholamini et al.., [10] proposed a design of 7:2 compressors. In this paper a new implementation for 7:2 compressors based on the conventional architecture is proposed. According to the results, the design presents achieves a remarkable improvement in terms of speed and power consumption. This accomplishment is the direct result of shortening the critical delay path.

Danapat A et al.., [11] proposed a 16×16 Bit Binary Multiplier using high speed compressors. For higher order multiplications, a huge number of adders or compressors are to be used to perform the partial product reduction. In this paper the number of adders is reduced by introducing special kind of adders that are capable to add five/six/seven bits per decade. These adders are called compressors. Binary counter property has been merged with the compressor property to develop higher order compressors. Use of these compressors permit the reduction of vertical critical paths. These compressors make the multiplier faster as compared to the conventional design.

Saleh Abdel-Hafeez et al.., [12] this paper presents a high speed wide range parallel counter that achieves high operating frequencies through a pipeline partitioning methodology (a counting path and state look ahead path), using only three simple repeated CMOS -logic module types: an initial module generates anticipated counting states for higher significant path. The power consumption, delay and area are discussed in this paper.

Mehdi Ghasemzadeh et al.., [13] proposed the fast glitch less 7-3 counter for a CMOS low power, high speed multiplier. In order to reduce delay and increase the speed, some changes have been made in the structure of the counters. Also, the occupied area by the counter is decreased because of the less number of transistors. For the proposed counter there is a low-delay from the input

Table 1. Comparison Table

S.No	Author	Technique	Advantage
01	Earl E. Swartzlander et al	Full adder, Fast adder and Quasi digital counters	Fast adder counters results in high speed
02	Hideaki Kobayashi et al	Synthesizing large parallel counters into smaller ones	Can handle a large number of inputs
03	Robert F. Jones etal	Design of a large parallel counter	Area and delay are reduced in (3,2) counter
04	Behrooz Parhami et al	Developing a parallel counter with a Generalization of sequential counter	Leads to significant reduction in complexity and delay
05	Shen-Fu Hsiao et al	Designing a parallel counter with Double Pass Transistor (DPL) logic	Internal node capacitance on the critical path is reduced
06	Zhaojun Wo et al	Saturating counters based on Threshold logic	Reduced delay in saturating counters
07	Sreehari Veeramachaneni et al	(m,n) parallel counters	High speed and efficient design
08	Krithi Krishna M et al	Designing of compressors using XOR/XNOR logic	Lesser delay due to combination of low power and low transistor count
09	Mahnoush Rouholamini et al	7-2 compressors based on conventional architecture	Shortening of critical delay path
10	Mehdi Ghasemzadeh et al	Glitch less 7-3 Counter	Low delay from inputs to outputs.
11	Christopher Fritz et al	Counters based on symmetric Stacking	Delay and power consumption are reduced

to the output. Therefore, these types of counter can be used in high multipliers to decrease the number of partial products.

Shahzad Asif et al.., [14] proposed different architectures of counters based Wallace multipliers. A number of modifications are proposed in the literature to optimize the speed and area of the Wallace multiplier. Six architectures are proposed in this paper such as the first one consists of only 2:2 compressors. The second one is designed to reduce the 2:2 compressors. The third one uses 2:2 and 3:2 compressors. The fourth one uses 2:2, 3:2 and 4:3 counters. The fifth one uses 2:2, 3:2, 4:3, 5:3 counters. The 7:3 and 6:3 counters are used wherever possible. The sixth architecture consists of only7:3 counters. The analysis says that counter based Wallace multipliers are faster as compared to the traditional Wallace multipliers.

Christopher Fritz et al.., [15] proposed a binary counter based on symmetric stacking. It uses 3- bit stacking circuits, which group all of the one bits together followed by a symmetric stacking method to combine pairs of 3-bit stacks into 6- bit stacks. The bit stacks are then converted to binary counts, producing 6:3 counter circuits with no XOR gates on the critical path. This avoidance of XOR gates results in faster efficient power and area utilization. In VLSI simulation, the proposed counters are 30% faster than the existing parallel counters and also consumes less power than other higher order counters.

3. CONCLUSION

From the analysis the counter based on symmetric stacking have the reduced delay power consumption when compared with the conventional counter techniques. The accompanying Table I list out the outcomes got by various systems. In symmetric stacking the 6:3 and 7:3 counters are designed which gives a 30% reduction in the delay and power consumption. The 6:3 and 7:3 counters are applied to the Wallace tree multipliers and a significant reduction in the delay and power consumption is obtained during the process of partial product reduction.

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