Design of Urdhava Triyakbhyam for FIR Filter

Y.Angelin Jasmine and C.Chitra

***Abstract*—Recently the DSP processor which requires the very high speed of operation. The DSP processors are depend on the mathematical concepts. FIR filter are often involved in VLSI signal processing and communication system. The basic structure of FIR filter have the block of addition, multiplication and delay element. In that, FIR filter the addition and multiplication which takes excess time thus minimize the speed of the processor. In this paper, we propose the technique which is efficient to improve the processor speed using ancient vedic sutras. The design of FIR filter using URDHAVA TRIYAKBHYAM it has ability to increase processor speed, reduce area and power.**

***Index Terms*— Half adder (HA), Full adder (FA), Special adder (SA), Finite impulse response (FIR), Vedic multiplier, Urdhava triyakbhyam.**

I. INTRODUCTION

In the discrete time signal by the digital hardware involves mathematical operations like addition, multiplication and time delay. The time taken to process the discrete time signal and the computational complexity depends on number of calculations involved in the type of arithmetic used for computation. In many digital signal processing applications FIR filters are preferred over their IIR filters. The word "Finite impulse response" is no feedback, impulse response is finite. Different multipliers are used to reduce area, time delay and speed.

High performance and low complexity design using the Multiple constant multiplication (MCM) technique offering for execution of FIR filters [1]. To mininimize the computational complexity the elimination of MAC unit by the horizontal and vertical sub expression method. In the reconfigurable FIR filter the area and delay are efficient. The rounded truncated multiple constant multiplication Structure [2] in FIR can be operated by truncated multipliers which is the development method; Mainly the faithfully rounded module to get the minimization in area and the power consumption. A reconfigurable filter is implement with low complexity which can be actively operated by common sub expression elimination algorithms [3]. The common sub expression elimination (CSE) methods depend on canonical signed digit (CSD) coefficients which produce low complexity FIR filter coefficient multipliers. Also, a Constant shifts method (CSM) and Pulse shift method (PSM) are implementing a reconfigurable filter with low complexity.

A new distributed arithmetic formulation is to perform [4] a block least means square (BLMS) algorithm. DA-based design which is used in a novel look-up table (LUT) to sharing method for the computation and weight-increment terms of BLMS algorithm. It allows to reduce area, time complexity and power. Error-compensated adder-tree (ECAT) [5] based on the truncation errors and to get low-error and high-throughput discrete cosine transform (DCT) The requirements of PSNR DA which has 9 bits as a replacement of 12 bits. The highest hardware efficiency in the DCT which needs same PSNR requirements. Fixed-width multipliers that gives an -bit product [6]. These method has four steps to get improved error-compensation. The error-compensation can be mapped to low-error and area-efficient fixed-width multipliers applicable for VLSI implementation and DSP application. FIR filter determines with power simulations, by providing [7]the perturbation of the coefficients of baseline filters to reduced power consumption of the filter. The Booth recoding is fast multiplier. The PPR providing a lower critical path. Pseudo-carry compensation truncation (PCT) with array multiplier [8] based on the truncated array multipliers as much as 25% of silicon area and delay, and consumes about 40% less dynamic power operation. The mean square errors (MSE) is applied to an image compression algorithm.

The mean square error, [9] is a the partial-products of the chip. A sub-optimal compensation function, best suited for hardware implementation, be obtained as a linear combination of the terms. Truncated multipliers with the linear compensation function has been investigated. It has been shown that the proposed truncated multipliers can easily be realized by using a carry-save reduction tree followed by a final carry-propagate adder.

II. DESIGN A FIR FILTER USING URDHVA TRIYAKBHYAM SUTRAS

The addition, multiplication and signal delay are needed to design FIR filter. The huge amount of time is taken in another multiplier. Thus, increase the area of the design.

Vedic mathematics is used to increase the speed of the processor. URDHAVA TRIYAKBHYAM sutra is used for the fast multiplications.

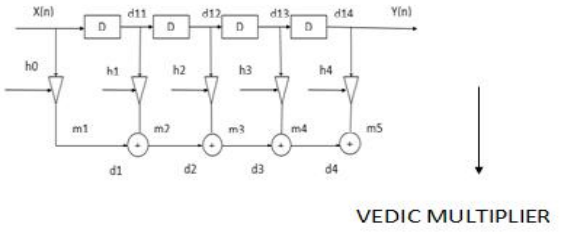

Fig. 1. Block diagram of a direct-form of FIR filter with vedic multiplier

The FIR filter is designed with Urdhva Tiryagbhyam sutra has a partial product. Vedic multiplier has a carry-skip technique. The various types of multiplication methods are available but this sutra is suitable for algorithms thus minimize the time delay.

The different multiplication are array, Wallace tree, Baugh wooley and booth multiplier but the fastest multiplier is Vedic. Vedic Mathematics which is widely used in ALU, MAC etc and produce efficient results. It reduce the complex calculation into easier for human mind calculations. Sixteen Sutras are designed by Vedas the 14th sutra is URDHAVA TRIYAKBHYAM sutra applicable for all mental calculations.

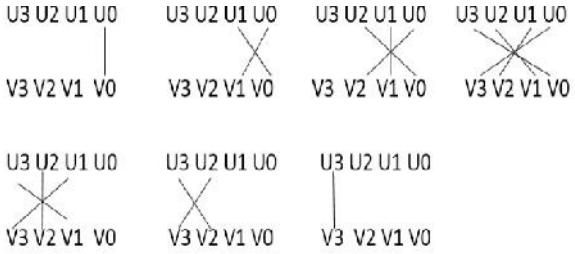

Fig. 2. Line diagram of Urdhva Tiryakbhyam Sutra for 4 x 4 binary number multiplication

.

Urdhva Tiryakbhyam refers to vertical and crosswise. Vertical refers to straight line and crosswise refers to diagonal multiplication. The number of steps based on the number of digits. The digits are the two lines which is given below. The 4*4 multiplier has input as U0,U1,U2,U3 and V0,V1,V2,V3. In the initial step U0 and V0 are multiplied with each other and result is added to the previous carry and further crosswise multiplication takes place and at last least significant digit is taken as result and other digits are consider as carry digit and it is neglected. It can be written as

T0=U0V0

T1=U1V0+U0V1
T2=U2V0+U1V1+U0V2
T3=U3V0+U2V1+U0V3
T4=U3V1+U2V2+U1V3
T5=U3V2+U2V3
T6=U3V3

The result can be obtained as T6T5T4T3T2T1T0. These sutras which is mainly used to reduce power and area.

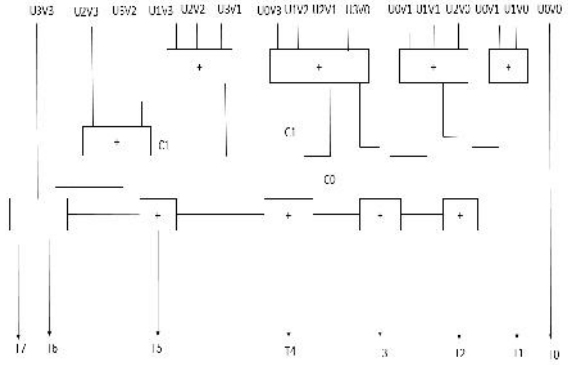

Fig. 3. Proposed Vedic multiplier architecture

The Vedic multiplier is coded by HDL (Hardware Description Language).It consists of 7 FA, 2 HA and 1 SA. The special adder has one sum and two carry C0 and C1. The main operation of special adder is used to minimize the time delay.

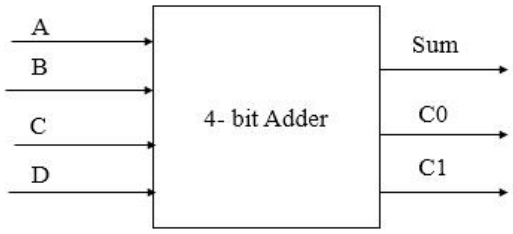

Fig. 4. Block diagram of 4 bit special adder

In the figure 4 A, B, C, D are four inputs. C0 and C1 are LSB and MSB of carry outputs respectively and Sum is the sum of four inputs. The Boolean expressions for the same are given below.

Sum= A XOR B XOR C XOR D
C0=((NOT B) AND D) OR (C AND (NOT D)) OR (B AND (NOT C))
C1=A AND B AND C.

In the line diagram of Urdhva Tiryakbhyam Sutra the U and V are the two 4 bit binary which consist of the AND gate , Half adder, Full adder and Special adder are used for these multiplications. For example the two 4 bit numbers 0001 and 0010 which get the output as

00000010. Here the previous carry must be consider to add with next step.

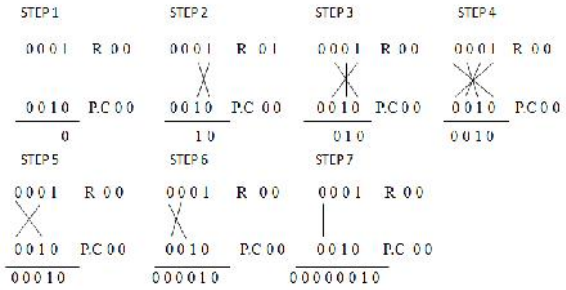

Fig. 5. Multiplication of two 4 bit binary number 0001*0010

These fast multiplier is applied to the FIR filter where input X(n) is 000001, h0 is 00101, h1 is 00100, h2 is 00011, h3 is 00010 and h4 is 00001. The equation can be written as

m1=X(n)*h0

=000001*00101 = 00000101

m2=z^{-1}X(n) ∗ h1

= 000001*000001*00100 =00000100

d1=m1+m2

=00000101+00000100 =0001001

m3=z^{-1}X(n) ∗ h2

=00000011

m4=z^{-1}X(n) ∗ h3

=00000010

m5=z^{-1}X(n) ∗ h4

= 00000001

d2=d1+m3 =0001100

d3=d2+m4 =0001110

Y(n)=d3+m5

Y(n) = 0000000000001111

The output of the FIR filter Y(n) is 0000000000001111. While applying the vedic multiplier it consume low power and the area is reduced.

III. SIMULATION AND RESULTS

Finally, the FIR filter with Vedic multiplier was designed. This block diagram is used to reduce time delay, area and power. The proposed design which was coded by HDL and designed by ISIM using Xilinx ISE 12.1. The clock signal which is applied as 0 or 1. The two 4 bit are multiplied the U and V are the inputs as 0001 and 0010 and get the output as 00000010 in fig 5.

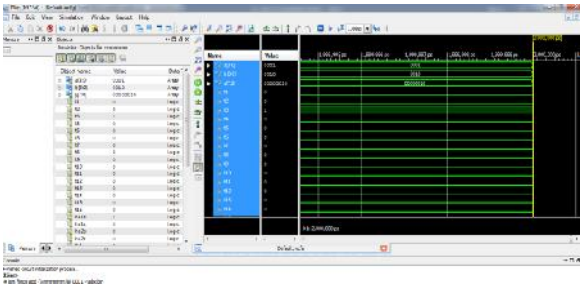

Fig. 5. Simulation of vedic multiplier

The simulation output for the proposed FIR filter is shown in the figure 5. The co-efficient are given as 101, 100, 011, 010, 001.The input is given as 0001 and get the output as 0000001111. The simulation results show that the Area, Power, Speed also Delay. The table 1 shows that the power, device utilization and timing consumption of the FIR filter using booth and vedic multiplier. In the design a FIR filter with booth recoded multiplier has the number of 4 input IoBs as 144 , time as 13.36ns and power as 1.06W and the design a FIR filter with vedic multiplier has the number of 4 input IoBs as 25, time as 11.91ns and power as 0.227W. As compare to the design of FIR fiter with booth recoded multiplier which has lower area, power ,time and higher speed of processor in the design of FIR filter with vedic multiplier.

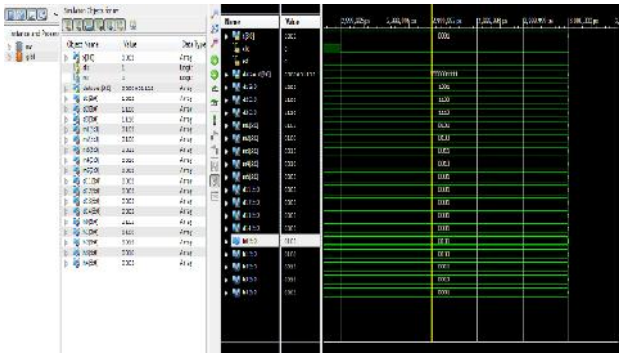

Figure 6: Simulation output of proposed FIR filter

The power can be calculated by using Xilinx Power Estimator(XPE). Comparison of power, delay time and LUT count of the proposed diagram. From table 1 the

proposed method helps to reduce LUT count, time delay and power.

Table 1: Comparison result of [10] and proposed FIR filter

Reference	LUT Counts	Time delay(ns)	Power(W)
[7]	144	13.36	1.063
Proposed	25	11.91	0.227

IV. CONCLUSION

Finally, the design of FIR filter using Vedic multiplier was designed. The complexity of the design is reduced than the booth recoded multiplier. The speed of the processor is increased in the DSP based application. In the Vedic multiplier Urdhava Triyakbhyam sutra is used for the simple mathematical calculations. The proposed block diagram in terms of area, time delay and power was compared with existing FIR filter which is reduce as 82.63%,10.85% and 78.64%.

Y.Angelin Jasmine, (PG Scholar)
Dr.C.Chitra M.E.,Ph.d., (Professor)
Dept. of ECE, PSNA CET
Dindigul, India.
(email ID:angelinyuvi@gmail.com)

REFERENCES:

[1] Basant Kumar Mohanty, Pramod Kumar Meher, "A high-performance fir filter architecture for fixed and reconfigurable applications", IEEE Transaction on VLSI system, Vol. 24, NO. 2, Feb 2016.

[2] Shen-Fu Hsiao, Jun-Hong Zhang Jian, Ming-Chih Chen, "Low-cost fir filter designs based on faithfully rounded truncated multiple constant multiplication / accumulation", IEEE Transaction on circuits and systems,2013.

[3] R. Mahesh, A. P. Vinod, "New reconfigurable architecture for implementing fir filters with low complexity", IEEE Transaction on computer-aided design of integrated circuits and systems, Vol. 29, No. 2, Feb 2010.

[4] Basant K.Mohanty, Pramod Kumar Meher, "A high-performance energy-efficient architecture for FIR adaptive filter based on new Distributed Arithmetic Formulation of Block LMS algorithm", IEEE Transaction on signal processing, Vol. 61, No. 4, February 15, 2013..

[5] Yuan-Ho Chen, Tsin-Yuan Chang, Chung-Yi Li, "High throughput DA-based DCT with high accuracy error-compensated adder tree", IEEE Transaction on VLSI system, Vol.19 N0.4 ,April 2011.

[6] Lan-Da Van,Chih-Chyau Yang, "Generalized low-error area efficient fixed width multipliers",IEEE Transaction on circuits and systemVvol.52, No.8 August 2005.

[7] Andrea Bonetti, Adam Teman, Flatresse, Andreas Burg, "Multipliers-driven perturbation of coefficients for low-power operation in reconfigurable fir filters", IEEE Transaction on circuits and system,2017.

[8] Chip-Hong Chang , Ravi Kumar Satzoda, "A low error and high performance multiplexer-based truncated multiplier", IEEE Transaction on VLSI system, Vol.18, No.12,Dec 2012.

[9] Nicola Petra, Davide De Caro, "Truncated binary multipliers with variable correction and minimum mean square error", IEEE Transaction on circuits and system Vol.57, No.6 August 2010.