Multiple Cell Upset Tolerant Error Detection and Correction Code for Semiconductor Memories using DSSC

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Abstract: Errors that affect memories are a major issue in advanced electronic circuits. As technology scales, multiple bit errors become more likely. This limits the applicability of traditional protection techniques like Matrix code or single error correction codes that can correct only one error. Multiple errors tend to affect adjacent bits, and therefore it is interesting to use error correction codes that can correct adjacent errors. The issue with these codes is that they require a large area and delay that limits their use to protect flip-flops in circuits. This project presents the implementation and evaluation of the Data Segmentation Section Code (DSSC), a new algorithm for the detection and correction of multiple transient faults in volatile memories with low cost implementation. .our proposed system has been coded in Verilog HDL and simulated using Xilinx 12.1.

Keywords: Xilinx, Verilog, DSSC

I. INTRODUCTION

Error detection is the detection of errors caused by noise or other impairments during transmission from the transmitter to the receiver. Summer is another name for error detection. Error correction is the detection of errors and reconstruction of the original, error-free data.

The general idea for achieving error detection and correction is to add some redundancy (i.e., some extra data) to a message, which receivers can use to check consistency of the delivered message, and to recover data determined to be corrupted. Error-detection and correction schemes can be either systematic or non-systematic: In a systematic scheme, the transmitter sends the original data, and attaches a fixed number of check bits (or parity data), which are derived from the data bits by some deterministic algorithm. If only error detection is required, a receiver can simply apply the same algorithm to the received data bits and compare its output with the received check bits; if the values do not match, an error has occurred at some point during the transmission. In a system that uses a non-systematic code, the original message is transformed into an encoded message that has at least as many bits as the original message.

II. RELATED WORKS

1) Punctured Difference Set (PDS) codes have been used to deal with MCUs in memories.
2) Interleaving technique has been used to restrain MCUs , which rearrange cells in the physical arrangement to separate the bits in the same logical word into different physical words.
3) Built-in current sensors (BICS) are proposed to assist with single-error correction and double-error detection codes to provide protection against MCUs
4) 2-D matrix codes (MCs) are proposed to efficiently correct MCUs per word with a low decoding delay, in which one word is divided into multiple rows and multiple columns in logical. The bits per row are protected by Hamming code, while parity code is added in each column.

Drawbacks:

1) PDS codes require more area, power, and delay overheads since the encoding and decoding circuits are more complex in these complicated codes.
2) Interleaving technique may not be practically used in content-addressable memory (CAM), because of the tight coupling of hardware structures from both cells and comparison circuit structures
3) BICS technique can only correct two errors in a word.

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4) 2D MC is capable of correcting only two errors in all cases.

In the recent technique names as FUEC–triple adjacent error correction (TAEC), is able to correct an error in a single bit, or an error in two adjacent bits (2-bit burst errors) or a 3-bit burst error, or it can detect a 4-bit burst error. This is possible by adding one more code bit. In this case, for a 16-bit data word, the FUEC–TAEC code needs eight code bits. The parity-check matrix **H** for this code is presented. As in the case of the FUEC–DAEC, *Ci* are the code bits and *Xi* are the primary data bits. Similarly, from **H** it is very easy to design the encoder/decoder circuitry. But this technique will be considered as less precision which could not correct the large number of datas.

III. PROPOSED SYSTEM

In this paper, we proposes a new algorithm named as Data Segmentation Section Code (DSSC)) based on divide-symbol is proposed to provide enhanced memory reliability. This algorithm for the detection and correction of multiple transient faults in volatile memories with low cost implementation.

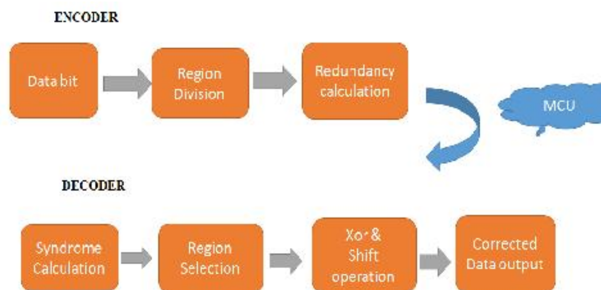

Fig.1 Proposed architecture

DSSC is an ECC based on two-dimensional (2D) codes, such as that aims to correct and detect MCUs in memories. The code presented in this paper codifies 16 data bits in 32 bits. However, only parity bits are used in encoding data bits to reduce the cost of implementation.

DSSC Encoding Process

Fig.2 shows the structure of 32 bits of data encoded by DSSC. The cells shaded in gray are the data bits, which were divided into four groups (A, B, C, D), each group with four bits.

A_1	A_2	A_3	A_4	Di_1	Di_3	CbA_{13}	CbA_{24}
B_1	B_2	B_3	B_4	Di_2	Di_4	CbB_{13}	CbB_{24}
C_1	C_2	C_3	C_4	P_1	P_3	CbC_{13}	CbC_{24}
D_1	D_2	D_3	D_4	P_2	P_4	CbD_{13}	CbD_{24}

Fig.2 DSSC Encoded data model.

The cells shaded in green are the *Diagonal bits* (D_i) calculated with XOR operations (xor) in specific data bits:

$$Di_1 = A_1 \oplus B_2 \oplus C_1 \oplus D_2$$

$$Di_2 = A_2 \oplus B_1 \oplus C_2 \oplus D_1$$

$$Di_3 = A_3 \oplus B_4 \oplus C_3 \oplus D_4$$

$$Di_4 = A_4 \oplus B_3 \oplus C_4 \oplus D_3$$

The cells shaded in blue are *Parity bits* (P) calculated with XOR operations in the data bits columns:

$$P_1 = A_1 \oplus B_1 \oplus C_1 \oplus D_1$$

$$P_2 = A_2 \oplus B_2 \oplus C_2 \oplus D_2$$

$$P_3 = A_3 \oplus B_3 \oplus C_3 \oplus D_3$$

$$P_4 = A_4 \oplus B_4 \oplus C_4 \oplus D_4$$

The cells shaded orange are *Check bits* (Cb) calculated with XOR operations in interleaved bits of each group:

$$CbA_{13} = A_1 \oplus A_3$$

$$CbA_{24} = A_2 \oplus A_4$$

$$CbB_{13} = B_1 \oplus B_3$$

$$CbB_{24} = B_2 \oplus B_4$$

$$CbC_{13} = C_1 \oplus C_3$$

$$CbC_{24} = C_2 \oplus C_4$$

$$CbD_{13} = D_1 \oplus D_3$$

$$CbD_{24} = D_2 \oplus D_4$$

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After the calculation of the redundancy bits, the encoding process ends and the 32 bits can be stored. Note that the Di bits and Cb bits are positioned between the data bits and Cb bits, in order to improve the efficiency of DSSC against MCUs characterized by adjacent error patterns. Figure describes the mains elements of the parity operation of the DSSC encoder.

The decoding process of DSSC is divided into three steps:

Syndrome estimation of the redundancy bits - The syndrome estimation consists of a XOR operation between the redundancy data stored and the recalculated redundancy bits (RDi, RP, and RCb). Therefore, the values for the Syndrome of Diagonal (SDi), Parity (SP) and Check bits (SCb) are estimated by:

$$SDi = Di \oplus RDi$$

$$SP = P \oplus RP$$

$$SCb = Cb \oplus RCb$$

Verification of error decoding conditions - After the calculation of the Syndromes, one of these two conditions need to be satisfied before the error correction execution: (i) both SDi and SP vectors must have at least one value equal to one; (ii) more than one SCb value is equal to one. These conditions allow the algorithm to detect an error in the data bits region. Their applicability will be explained with more details subsequently.

Selection of the wrong data region and correction process - In this phase of the decoding process, a specific region of the data bits is selected to be corrected. These regions are divided as it shows in the below Figure (a), (b) and (c). The proposal in split the data bits in three regions was elaborated in order to select a specific group of bit to operate the correction process. This approach reduces considerably the area and power cost.

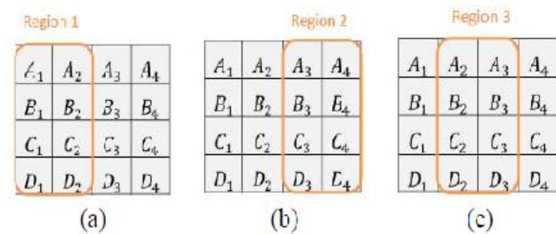

Fig.3 Regions of data bits.

The fig 3(a), (b) and (c) show that region 1, 2 and 3 are formed by data bits distributed in columns (1 and 2), (3 and 4) and (2 and 3), respectively. The selection of which region will be corrected is defined by the integer sum (+) of specific bits of SDi and SP. Table presents a group of equations which describes the criterion for region selection of DSSC, where the region with more syndrome bits equals to 1 is be declared as the wrong one (Region 1 or Region 2). If the sum of the equations presents equal value, then the Region 3 is selected.

Table1 : Region selection criterion.

Region selected	Criterion to selection
Region 1	$(SDi_1 + SDi_2 + P_1 + P_2) > (SDi_3 + SDi_4 + P_3 + P_4)$
Region 2	$(SDi_1 + SDi_2 + P_1 + P_2) < (SDi_3 + SDi_4 + P_3 + P_4)$
Region 3	$(SDi_1 + SDi_2 + P_1 + P_2) = (SDi_3 + SDi_4 + P_3 + P_4)$

For regions 1 and 2, the correction procedure consists in a XOR operation between the region selected and the SCbs matrix. Region 3 is a special case where it is strictly necessary that neither of all SDi and SP bits are null, even if the condition II of step 2 is satisfied. Note that Region 3 has its first column formed by values with the even index (2), meaning that the correction performed has to be different from the other regions. If region 3 is selected, the correction procedure must be performed by SDi with shifted positions, to align the indexes of SCbs with the matrix of Region 3. In the following section, some correction examples performed by the proposed method are described. Figure summarizes the operation performed by the decoder described in this section.

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IV. EXPERIMENTAL RESULTS

The proposed circuit are simulated and synthesized by using modelsim and xilinx12.1 which occurs low area than the existing. The experimental results are given in Table2 and the simulation results of layout and the waveforms are shown in the fig.4 and 5. Then the synthesis result of the proposed are shown in fig.6.

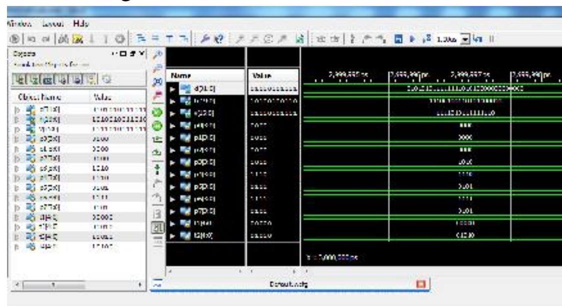

Fig.4 simulation results

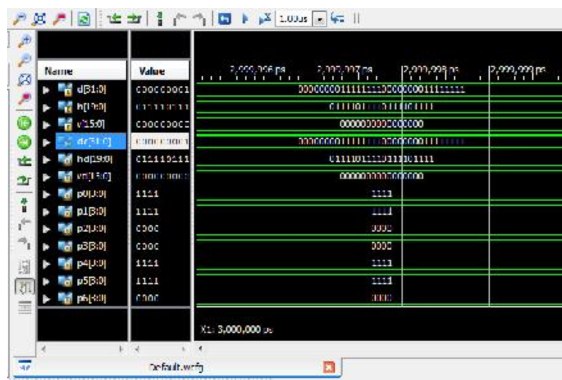

Fig. 5 output waveform of proposed

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Util
Number of Slices	29	960	
Number of 4 input LUTs	50	1920	
Number of bonded IOBs	47	83	

Fig.6 synthesis report of proposed architecture

Table 2: comparison of existing and proposed results

S.No	Parameter	Existing	Proposed
1	Slice	56	29
2	LUT	96	50
3	IOB	39	47

V. PERFORMANCE ANALYSIS

The Figure given below is shown that there is a considerable reduction based on no of transistors and the performance chart has been shown below in fig.7

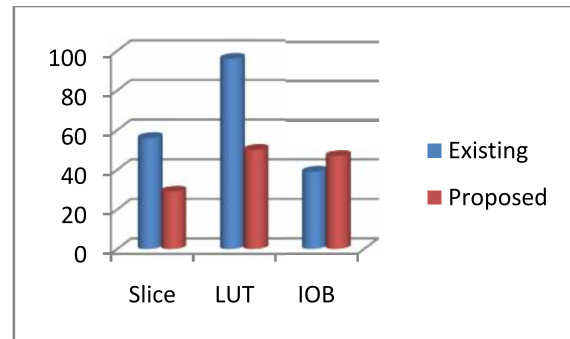

Fig.7 performance analysis

VI. CONCLUSION

This project proposes Data Segmentation Section Code (DSSC) an error detection/correction code for memory devices subjected to multiple cell upsets (MCUs). This code is based on parity codes and interleaving to deal with several patterns of MCUs. DSSC showed up as the lowest cost code of all evaluated codes. The utilization of Hamming and Extended Hamming in the ECCs Matrix and CLC, respectively, brought advantages in what concern error coverage. However, this also increased heavily the cost of both codes when compared with DSSC. Regarding the experimental results, DSSC presents the best results for all fault scenarios , which means that DSSC has the better tradeoff between error coverage and implementation cost than all codes analyzed.

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