QCA Design of Encoder for Low Power Memory Applications

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Abstract: Quantum-dot fabrication and characterization is a well-established technology, which is used in photonics, quantum optics and nan electronics. Four quantum-dots placed at the corners of a square form a unit cell, which can hold a bit of information and serve as a basis for Quantum-dot Cellular Automata (QCA) nan electronic circuits. Although several basic QCA circuits have been designed, fabricated and tested, proving that quantum-dots can form functional, fast and low-power nan electronic circuits, QCA nan electronics still remain at its infancy. One of the reasons for this is the lack of design automation tools, which will facilitate the systematic design of large QCA circuits that contemporary applications demand. Here we present novel, programmable QCA circuits, which are based on crossbar architecture. These circuits can be programmed to implement any Boolean function in analogy to CMOS FPGAs and open the road that will lead to full design automation of QCA Nano electronic circuits. Using this architecture design and simulation of QCA circuits have proved to be area efficient, stable and reliable.

Keywords: QCA, CMOS FPGA, Quantum-dot

I. INTRODUCTION

THE increasing demand for low-power very large scale integration (VLSI) can be addressed at different design levels, such as the architectural, circuit, layout, and the process technology level. At the circuit design level, considerable potential for power savings exists by means of proper choice of a logic style for implementing combinational circuits. This is because all the important parameters governing power dissipation—switching capacitance, transition activity, and short-circuit currents—are strongly influenced by the chosen logic style. Depending on the application, the kind of circuit to be implemented, and the design technique used, different performance aspects become important, disallowing the formulation of universal rules for optimal logic styles. Investigations of low-power logic styles reported in the literature so far, however, have mainly focused on particular logic cells, namely full-adders, used in some arithmetic circuits.

VLSI fabrication process keep on shrinking the physical sizes down to atomic scale dimensions and the operational frequencies of terahertz can be easily obtained if the devices can operate with less no. of electrons. However, there is a need for a trade-off to be made between increasing requirements of performance parameters and the feature size. The eventual saturation of CMOS technology is not due to inability to reduce its physical size further, but the detrimental effects of quantum mechanical effects on tiny transistors. for e.g., In nanoscale transistors, impermissible amounts of current leaks due to such highly narrow channels and ultra thin insulating layers.

Nanotechnology is one of the possible alternatives to the stated trade off problem. ITRS report summarized several possible solutions. The possible variants are i) Deltt (double–electron-layer tunneling transistor) developed by scholars at SN labs, ii) SET (single electron transistors) iii) rapid single quantum flux logic, iv)quantum cellular automata. SET's are a promising technology for non volatile memory.

In this paper, Our main objective is programmable QCA circuits, which are based on crossbar architecture. These circuits can be programmed to implement any Boolean function in analogy to CMOS FPGAs and open the road that will lead to full design automation of QCA Nano electronic circuits. Using this architecture we designed and simulated QCA circuits that proved to be area efficient, stable and reliable.

II. RELATED WORKS

Dariush Abedi and Ghassem Jaberipur emerging technologies, with low area/power/latency properties, are gaining momentum as replacements for CMOS. In particular, for quantum dot cellular automata (QCA) realization, many arithmetic circuits have been redesigned. The basic QCA elements are a 3-way majority gate and an inverter. The trivial mapping of logical circuits to their QCA equivalents via direct replacement of AND and OR gates with partially utilized majority (PUM) gates (i.e., with a ‘0’ and ‘1’ input, respectively) leads to exploitation of QCA basic components.

Regarding the revitalized decimal arithmetic units in digital processors, researchers have begun to design decimal arithmetic circuits on QCA. For example, several QCA decimal full adders are trivially designed via the aforementioned direct mapping. However, only one proposition in the literature tries to make better use of majority gates, but yet replaces many AND and OR gates by PUMs. In this paper, we propose a QCA decimal full adder that is mostly composed of fully utilized majority gates (i.e., with no constant inputs), and rarely includes PUMs.

To introduce the novel architecture proposed for implementing ripple adders in QCA, let consider two n-bit addends A = an−1, . . . , a0 and B = bn−1, . . . , b0 and suppose that for the i th bit position (with i = n − 1, .. , 0) the auxiliary propagate and generate signals, namely pi = ai+ bi and gi= ai· bi , are computed. Ci being the carry produce dat the generic (i−1)th bit position, the carry signal ci+2,furnished at the (i+1)th bit position, can be computed using the conventional CLA logic reported. The latter can be rewritten as given in (3), by exploiting Theorems 1 and 2demonstrated. In this way, the RCA action, needed to propagate the carry ci through the two subsequent bit positions, requires only one MG. Conversely, conventional circuits operating in the RCA fashion, namely the RCA and the CFA, require two cascaded MGs to perform the same operation. In other words, an RCA adder designed as proposed has a worst case path almost halved with respect to the conventional RCA and CFA.

The design of the novel 2-bitmodule shown in Fig.1 that also shows the computation of the carry ci+1 = M(pi gi ci).

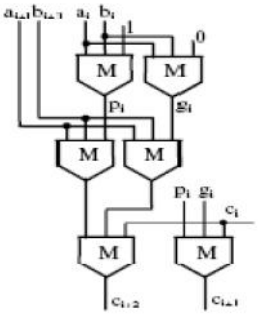

Fig.1. Novel 2-bit basic module.

This n-bit adder is then implemented by cascading n/2 2-bit modules as shown in Fig. 3.1. Having assumed that the carry-in of the adder is cin= 0, the signal p0 is not required and the 2-bit module used at the least significant bit position is simplified. The sum bits are finally computed as shown in Fig. (b).It must be noted that the time critical addition is performed when a carry is generated at the least significant bit position (i.e., g0 = 1) and then it is propagated through the subsequent bit positions to the most significant one.

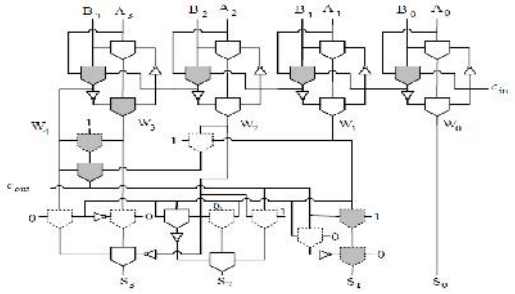

Fig.2. DFA with 16 fully- and 9 partially-utilized gates

Fig.2 presents a 28 M gate implementation of the latter described DFA, with 16 fully utilized versus 12 partially utilized (distinguished by dashed boxes) M gates. One drawback of this circuit is the long backward wires that are required in the paths for 1 and 2 (the thick lines). This leads to many crossovers (QX), which are hard to implement and degrade the circuit efficiency.

To remedy this problem, we propose the new equations 14 and 15, for 1 and 2 , respectively (with due justification to follow), where only the wire needs to be back warded. These new equations can be realized with 16 fully utilized and 9 partially utilized M gates.

$$
\begin{aligned}
s_1 &= c_{out} \oplus w_1 = (c_{out} \vee w_1)\overline{c_{out} w_1} \\
&= \mathcal{M}(w_1 \vee c_{out}, \overline{c_{out} w_1}, 0) \\
s_2 &= w_2 \oplus c_{out} \oplus (c_{out} w_1) = w_2 \oplus (c_{out} \overline{w_1}) \\
&= \overline{w_2} c_{out} \overline{w_1} \vee w_2 \overline{c_{out}\, \overline{w_1}} = \overline{w_1 w_2} c_{out} \vee w_1 w_2 \vee w_2 \overline{c_{out}} \\
&= \overline{w_1 w_2} c_{out} \vee w_1 w_2 (1 \vee c_{out}) \vee w_2 \overline{c_{out}} (1 \vee \overline{w_1}) \\
&= \overline{w_1 w_2} c_{out} \vee w_1 w_2 \vee w_1 w_2 c_{out} \vee w_2 \overline{c_{out}} \vee \overline{w_1} w_2 \overline{c_{out}} \\
&= \overline{w_1 w_2} c_{out} \vee \overline{w_1 w_2} s_2 \vee \overline{w_1} w_2 \overline{c_{out}} \vee \overline{w_1} c_{out} \overline{c_{out}} \vee \\
&\quad w_2 \overline{w_2 c_{out}} \vee w_2 c_{out} \overline{c_{out}} \vee w_1 w_2 \vee w_1 w_2 c_{out} \\
&= \overline{w_1 w_2} (c_{out} \vee w_2) \vee \overline{w_1 c_{out}} (c_{out} \vee w_2) \\
&\qquad + \overline{w_2 c_{out}} (c_{out} \vee w_2) \vee w_1 w_2 (w_2 \vee c_{out}) \\
&= (\overline{w_1 w_2} \vee \overline{w_1 c_{out}} \vee \overline{w_2 c_{out}})(c_{out} \vee w_2) \vee w_1 w_2 (w_2 \vee \\
&\quad c_{out}) \vee w_1 w_2 (\overline{w_1 w_2} \vee \overline{w_1 c_{out}} \vee \overline{w_2 c_{out}}) \\
&= \mathcal{M}\big((\overline{w_1 w_2} \vee \overline{w_1 c_{out}} \vee \overline{w_2 c_{out}}), (c_{out} \vee w_2), w_1 w_2\big) \\
&= \mathcal{M}(\overline{\mathcal{M}(w_1, w_2, c_{out})}, c_{out} \vee w_2, w_1 w_2)
\end{aligned}
$$

DRAWBACKS OF EXISTING SYSTEM

- Device density & interconnection.
- Circuit complexity.
- Physical limits.
- Non ideal effects.

III. PROPOSED APPROXIMATE ADDER

Our main objective is programmable QCA circuits, which are based on crossbar architecture. These circuits can be programmed to implement any Boolean function in analogy to CMOS FPGAs and open the road that will lead to full design automation of QCA Nano electronic circuits. Using this architecture we designed and simulated QCA circuits that proved to be area efficient, stable and reliable.

3.1 LOGIC GATES FOR QCA CROSSBAR CIRCUITS

Crossings of "horizontal" and "vertical" QCA cables type automated greater part gateways which have been developed and tested. QCA greater part checkpoint established at such a traversing. The gate consists of five tissues in each route. The three inputs to this checkpoint are the top, remaining and base tissues, A, B and C and the outcome is the right mobile. The outcome is equivalent to the majority of the feedback declares. The main mobile, which is the one that works the computations is known as the "device cell" and in every situation is in the same condition as the outcome. One of the three information of the greater part checkpoint can be used as a "program line". Let us believe, that this approach range comes in from the top feedback mobile, namely B, (of course any one of the feedback cell scan provide as a system range due to symmetry), and the rest of the two information cost nothing to be set at any condition. In such a case, one can see that if this approach range condition is set to one, the greater part checkpoint actually works the OR Boolean logic, while when this approach range is set to zero, the greater part gate becomes an AND checkpoint. Therefore, the greater part checkpoint can be programmed to function as an OR or an AND checkpoint by setting the condition of any one of its information to logic one or zero and keeping it continuous during the function of the checkpoint. Although QCA cable crossings can be developed to function as AND or OR gateways, they cannot be develop to function as NOT gates by establishing any two information to any logic value. The suggested technique is used to the style of a half-adder. As it is known, the half-adder routine consists of an AND and a XOR checkpoint. Using the suggested automated Boolean set, namely AND, OR and NOT, described previously, all other gateways are decomposed into the aforementioned gateways without any further lack of generality.

BLOCK DIAGRAM OF FULL ADDER QCA LAYOUT

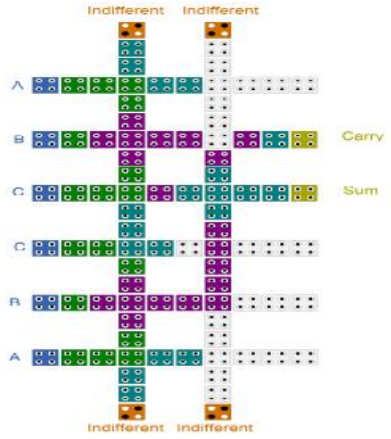

Fig.3 QCA Layout of Full Adder

In the process provided in this document, each routine under construction should contain only the primary gateways, namely the AND, OR and NOT gateways. Therefore, as described in previous section all other gateways are decomposed into the primary gates in purchase for the strategy to be applicable The logic routine of a full-adder using Majority gateways is shown in Fig We decides on this logic routine in order to show the versatility of the process. In more information, the circuit contains 3 Majority gateways and 2 inverters, whereas all 3input alerts of the 1-bit full-adder are placed into the circuit twice as provided.

IV. RESULT AND DISCUSSION

The layout of conventional full adder has 132 cells and the existing approximate adder has 112cells whereas the proposed approximate adder has only 27cells. So the cell count is reduced by a bigger margin thereby area is reduced. Simulation results window depicts the cell count. All the styles were confirmed using QCA Designer edition 2.3 . In the bistable approximation, we used the following parameters: mobile dimension = 18 nm, number of examples = 182 800, unity patience = 0.001000, distance of impact = 41 nm, relative permittivity=12.9, time high=9.8e−22, time low=3.8e − 23, time plenitude aspect = 2.000, layer

separation = 11.5000 nm, and highest possible iterations per example = 1000. The simulator outcomes of the Traditional one-bit QCA complete adder QCA layout caved has been verified using the QCA Designer device. QCA tissues are compared to the previously revealed styles.

Design	Existing count	Proposed count
Half Adder	92	50
Full Adder	160	92

Table1: comparison result of existing and proposed

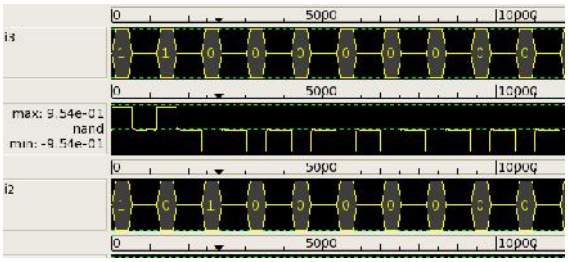

Fig.4 Simulation results

V. PERFORMANCE ANALYSIS

The Figure given below is shown that there is a considerable reduction in time and area based on the majority gates results which have been done by using QCA designer. The proposed algorithm significantly reduces area consumption when compared to the existing system(in fig.5).

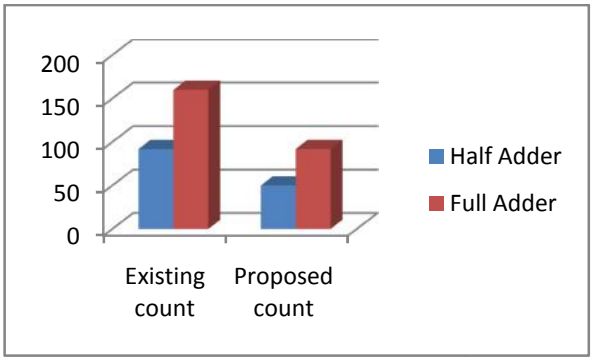

Fig.5 comparison chart

VI. CONCLUSION

Although QCA is a Nano electronic technology recognized as one of the top emerging technologies, its issues have not been adequately addressed and therefore, there is no consistent or standard framework in designing QCA circuits. Thus, in this paper, a novel design methodology aiming at implementing Boolean logic functions using programmable crossbar QCA circuits is presented. A similar QCA design methodology, to the best of our knowledge, does not exist in the literature. As an additional contribution, in the content of this work, a novel implementation of the QCA NOT gate is introduced facilitating the combination of the QCA nanotechnology with the crossbar architecture. This means that, the programmable AND and OR QCA gate in conjunction with the proposed QCA NOT gate can be implemented at a cross point of the crossbar and hence, to form a universal Boolean set suitable for designing any Boolean logic QCA circuit and implementing general computation. A Boolean reasoning feature using automated crossbar QCA circuits is provided. In summary, the suggested techniques generate size and weight effective tour. These elements of the proposed methodology along with its normalization, generality and programmability, are predicted to ensure it is very eye-catching to the designers.

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