Comparison of Latches and Flip-Flops in 45nm Technology

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Abstract- In this paper, commonly used latches and flip-flops are implemented is done in 45nm CMOS technology using Cadence tool. The aim behind the paper is to compare the power dissipated and delay in commonly used latches and flip-flops. Dlatch, Power PC603FF, TSPC based flip-flop and a dynamic double edge triggered flip-flop are simulated and power comparison is made. Power can be reduced by different low power techniques along with further tuning of width and length of the devices.

I. INTRODUCTION

Power consumption has become one of the major issues in VLSI design [1]. Power considerations have become important both from reliability point of view and also due to the advent of different portable battery driven devices. Designing low power devices is an issue in this scenario. For high performance VLSI design, latches and flip-flops have a great impact on power dissipation, speed and area of the circuit. Therefore, they are widely used in VLSI circuits. Latches and flip flops are the basic elements [2] and are used to store information and are the fundamental blocks of sequential circuits and these can be made from logic gates. A single flip flop and latch can store one bit of data. The main difference between the latches and flip-flops is that, a latch checks input continuously and changes the output whenever there is a change in input. But, flip flop is a combination of latch and clock that continuously checks input and changes the output time adjusted by the clock. Flip-flops and latches are circuit elements wherein its output not only depends upon current inputs but also previous inputs and outputs. A clocked latch is called a flip-flop. The major difference is the number of inputs it has and in which way they change their states.

Table 1 Comparison of latches and flip-flops

Latch	Flip-flop
It is transparent as input is directly connected to output when enable is high	It is a pair of latches (master and slave)
It is level triggered	It is edge triggered
Less area	More area
Less power	More power
It is based on the enable function input	It is based on clock pulse
It is sensitive to duration of pulse	It is sensitive to signal change

The main difference is in terms of triggering. Latch is level triggered which means the output of present state and input of next state depend on the level ,either a binary 0 or 1.On the other hand, flip-flop is edge triggered which means the output and next state input changes when there is a change in the clock pulse whether it is a positive or negative.
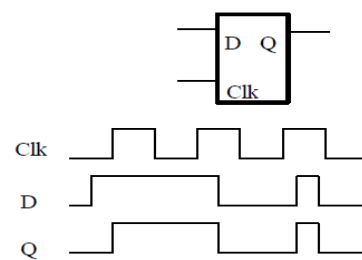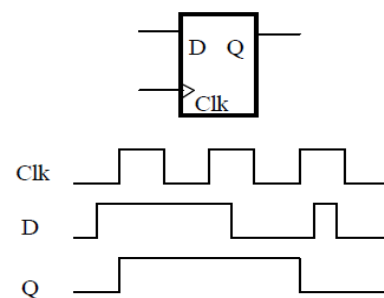

Fig.1.Output response of a latch

Fig.2.Output response of a flip-flop

Compared to flip-flop, latch is found to have more speed as longer path is compensated by shorter path delays in subsequent logic stages, but in flip-flops the delay is less than the clock period except for false and multi-cycle paths. As it results in the circuit performance negatively, designers rely on latch based designs. Design of few latches and flip-flops are simulated and analyzed in terms of power, area and propagation delay. They are:

[1] D latch
[2] PowerPC603 flip-flop
[3]TSPC based flip-flop
[4] DET D flip-flop

The main power consuming component in a VLSI circuit is the clock system that consists of clock allocation tree and register elements (latches and flip-

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flop)[1].For selection of any register elements, number of transistors, power, delay, better performance with low power and speed are the main parameters that must be considered. Power consumption of a clocking system can be represented as ,

$$P_{clksystem} = P_{clk-tree} + P_{register\ elements\ (flip-flop)} \qquad (1)$$

where, $P_{clk\text{-}tree}$ and $P_{register\ elements}$ in equation(1) represents power consumed by clock allocation tree and register elements respectively. The power consumed by clock tree is given as [1],

$$P_{clk-tree} = \{(C_{line} + C_{clk-tsr})V_{clk-swing}^2\}.f_{clk} \qquad (2)$$

where, C_{line} is the interconnect line capacitance, $C_{clk\text{-}tsr}$ is the capacitance of clocked transistors of the register elements and $V_{clk\text{-}swing}$ is the clock swing voltage in equation(2).The power consumed by the register elements can be expressed as,

$$P_{reg.elements} = \{(\alpha_i c_i \beta + \alpha_0 c_0 \beta + C_{clk-Buf)}.V_{DD}^2\}.f_{clk} \quad (3)$$

where α_i and α_o are the switching activity ratio of input and output node, c_i is the internal node capacitance of the register element, c_o is the output capacitance of the register element, $C_{clk\text{-}Buf}$ is the capacitance of the clock buffers inside the register elements, f_{clk} is the clock frequency and β is the trigger factor(1 for single-edge triggered flip-flops and 2 for double-edge triggered flip-flops) in equation(3).It is essential to reduce the power consumption in both clock allocation tree and register elements.

II. D latch

The D latch with enable input is shown in fig.1[3].When input is 1, output follows the input D. When input is 0, latch is disabled and output follows the previous value which is independent of input.

III. Power PC 603 FF

It is one of the most efficient static flip-flop architectures and is suited for WSN (Wireless sensor nodes) applications. A low power keeper structure combined with a low latency direct path adds to the merits of the design. It has no dynamic nodes and with the usage of transmission gates, it leads to low power consumption [4]. Only disadvantage is circuit has large delay due to the positive setup time, so it has moderate speed.

IV. TSPC based flip-flop

It is one of the most power efficient dynamic flip-flops in which only one transistor is clocked by short pulse train and hence the name 'True single phase clock'[5].It is a positive edge triggered flip-flop and it uses a single clock for synchronization.When clk is low,input gets isolated from output.The output will latch the complement of input when clock makes atransition from low to high.

V. DET DFF

It is one of the double edge triggered dynamic flip-flops proposed by Gago in [6].It has few number of transistors to maintain maximum excursion logic and to get a better level of immunity to metastabilty problems. It suffers from large clock load at the same level of performance as in case of a single edge triggered flip-flop.

Table.2.Performance comparison of latches and flip-flops

Architecture	Delay(ms)	Power dissipation(nw)
Dlatch	72.9	181.8
Power PC603FF	56.9	365.7
TSPC FF	8.8	72.7
DET DFF	120.93	156

VI. CONCLUSION

In this paper,few register elements(latches and flip-flops)are simulated in Cadence Virtuoso tool using 45nm CMOS technology and comparison has been performed in terms of power dissipation and delay. Latches require more tool manipulation and calculation to check its timing compared to flipflops which are easy to check its design using static timing analysis.High speed microprocessor design includes master-slave latches as logic can be added between rising and falling edges of clock.The most commonly used flipflop is data or delay flipflop.Care must be taken that level sensitive latches must not be included in FPGA. Both latches and flip-flops are the fundamental units in VLSI design. A designer must know how to utilize the time-borrowing ability of a latch for balancing slack while optimizing critical paths in design. To avoid unstable states in design, enable signal in latch must be stable. Power can be reduced further by different low power techniques combined with further tuning of width and length of the both latches and flip-flops.

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References

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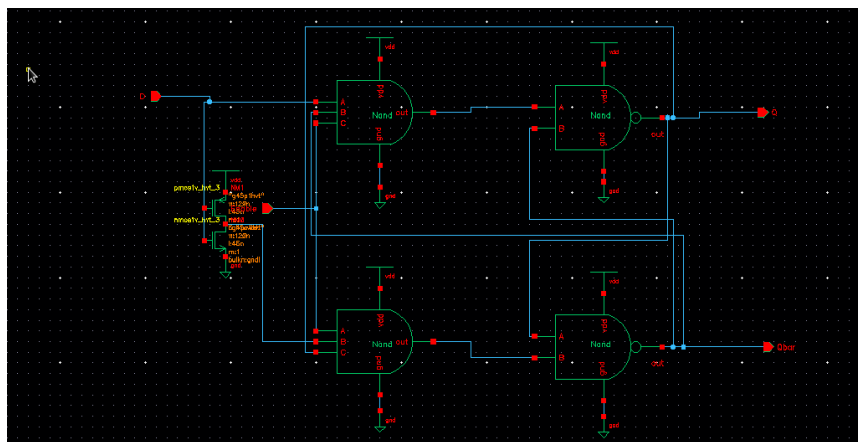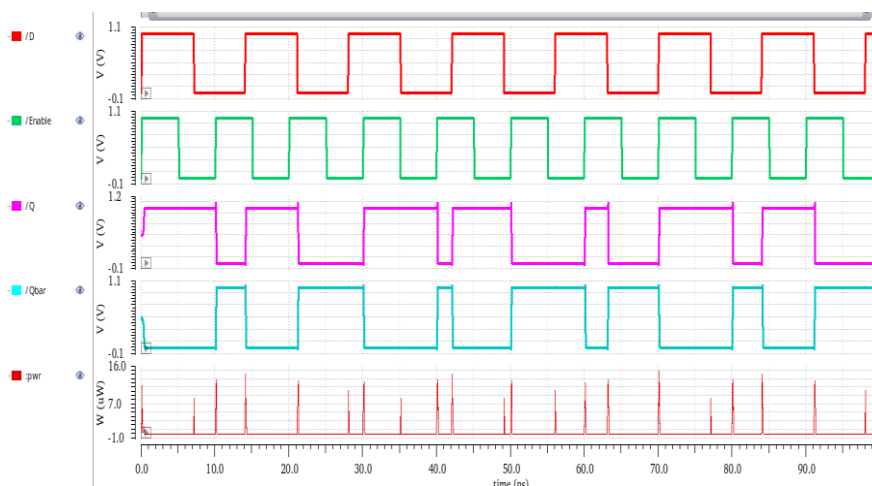
Annexure:

Fig.3.Schematic of D latch
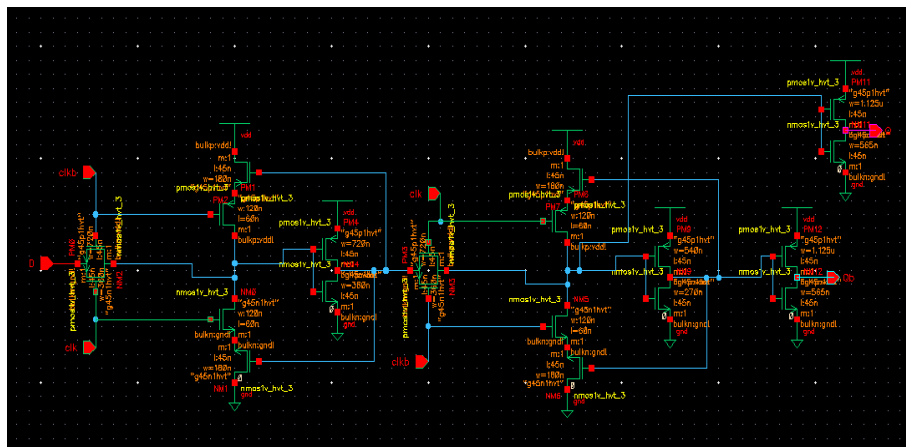

Fig.4.Output response of D latch

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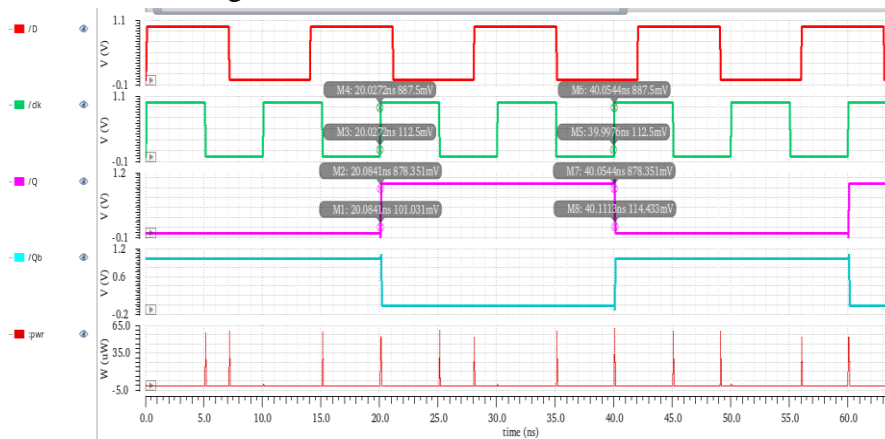Fig.5.Schematic of PowerPC603 FF[4]

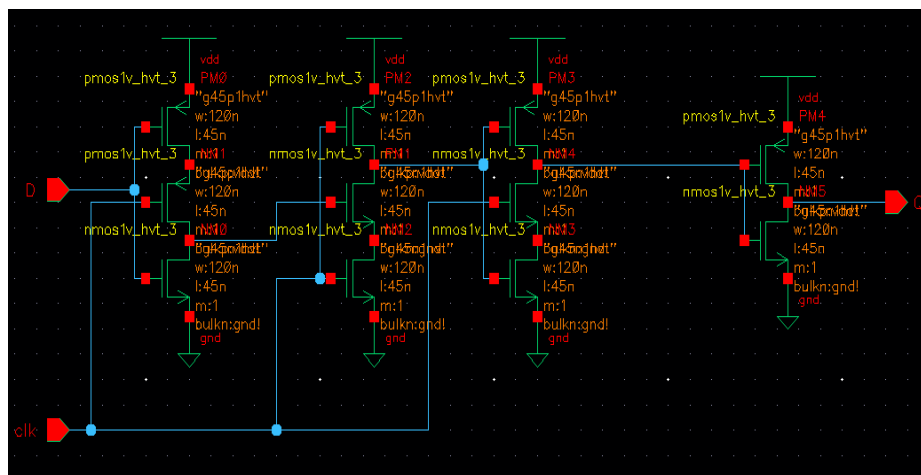
Fig.6. Output response of PowerPC603FF[4]

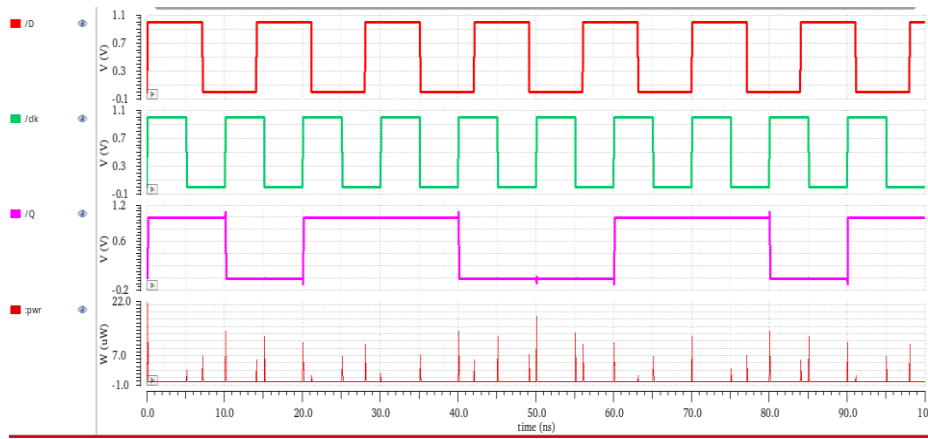Fig.7.Schematic of TSPC based flip-flop[5]

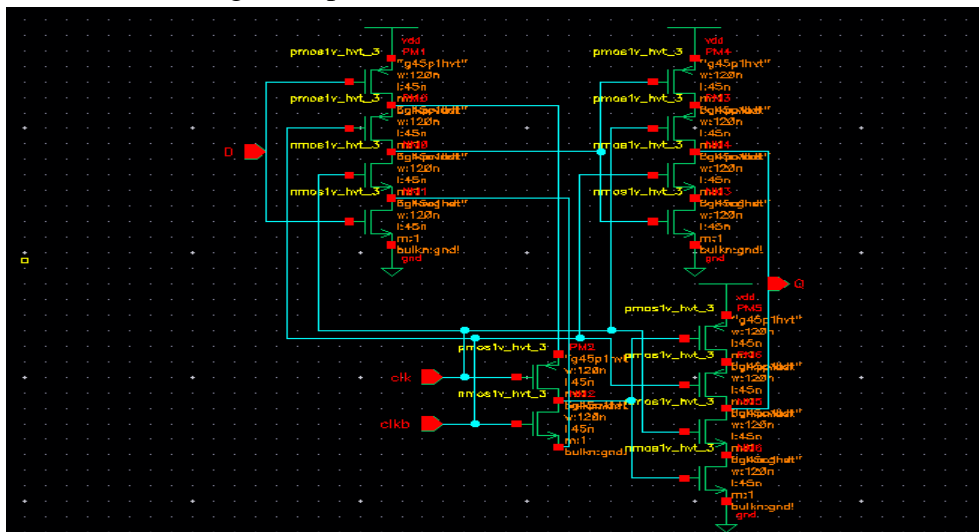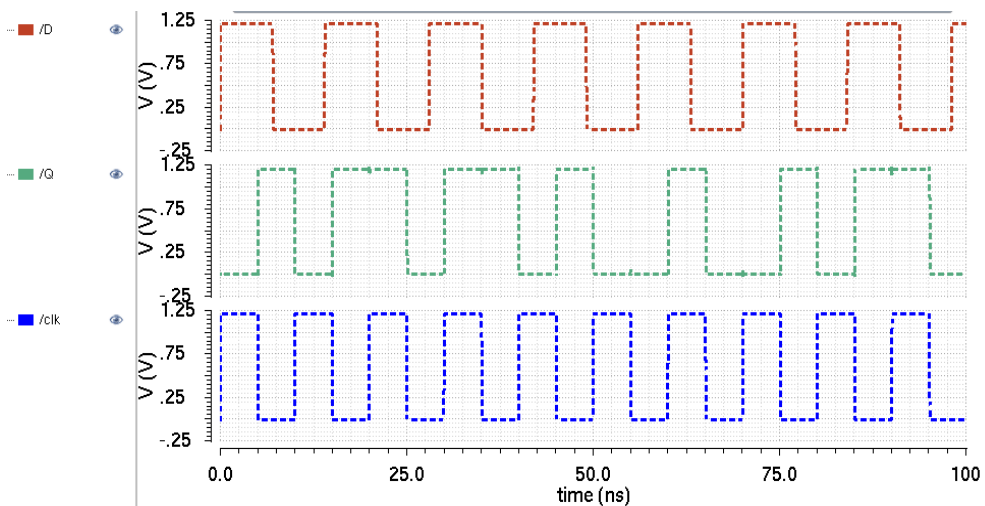Fig.8.Output waveform of TSPC based FF[5]

Fig.9.Schematic of DETFF[6]

Fig.10.Output waveform of DETFF[6]