FUZZY BASED DUAL-T-TYPE MULTILEVEL INVERTER FOR PHOTOVOLTAIC POWER SYSTEM APPLICATIONS

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ABSTRACT—

The switched-capacitor-based cascaded multilevel inverters (CMI) have been emerging due to their voltage boosting capability. Unfortunately, they suffer from impulse charging current and nonuniform operation. This project presents a topology termed as dual-T-type five-level CMI for photovoltaic power system applications, to resolve these problems without compromising the desirable voltage boosting characteristic. The main idea is to integrate a half bridge and an inductor to soft charge a capacitor that is connected in series with the dc source. The capacitor enables the voltage gain boosted to two, while the control of eight power switches that constitutes a dual-T structure enables five voltage levels generation. This solar based dual-T-type five-level CMI topology is control by using fuzzy logic controller. In addition, uniform operation is achieved for cascaded extensions. The operating principle of the proposed topology is analyzed and elaborated. For validation and simulation results of a prototype are presented using MATLAB Simulink platform.

I - INTRODUCTION

In the last decades, multilevel inverters have been extensively researched in view of the continuous development of power devices and the fast growing need for emerging applications such as micro grid. The conventional topologies, i.e., neutral-point-clamped inverter, flying capacitor inverter, and cascaded H-bridge (CHB) inverter have been proven as mature solutions for industrial applications. However, this does not hinder continuous research effort in contributing new promising topologies to offer wider possibilities in multilevel inverter technology.

Being one of the most well-established multilevel inverters that has been successfully commercialized, CHB inverter stands out due to its attractive modularity feature. Significant interest has been garnered in the development of alternative modules in place of H-bridge for improved performance.

To date, various types of cascaded multilevel inverters (CMI) have been proposed in literature. Most of them are based on the concept of switched dc source, where each of its isolated dc source is controlled by a half bridge to generate unipolar voltage levels across the dc link. Bipolar output voltage is achieved by controlling an H-bridge connected across the dc link. This topology is therefore termed as multilevel dc-link inverter. In a similar topology, a T-type inverter has been proposed as a replacement for the H-bridge.

In the recent works, considerable attention has been focus on developing cascaded modules by utilizing T-type inverter. A slight modification can further increase the number of levels to 17 by replacing the half bridge with a T-type inverter to constitute a two back-to-back T-type inverters structure. Despite not being mentioned in the literature, it is found that the ratio of asymmetrical dc sources is extended from $2V$dc:Vdc to $3V$dc:Vdc, which aggravates the power balancing issue. Similar topologies based on back-to-back T-type inverters are also presented. The module can be extended by enclosing more T-type inverters. Alternatively, proposes to extend the module to a switch-ladder structure by connecting more dc sources in series. Optimal design of this topology has validated its lowest power switch count compared to other cascaded modules. While the freewheeling current during dead-time commutation is not taken into account in the design, this topology is suffering from voltage spikes during transition between voltage levels.

All the aforementioned modules require the same number of dc sources as that in CHB due to their limited voltage gain. To address this problem, switched-capacitor (SC) based CMI (SC-CMI) are established. Self-voltage balancing and voltage boosting are two distinctive benefits of SC-CMI. The former is achieved by charging the SCs in parallel with the dc source, while the latter is achieved by discharging the SCs in series with the dc source. However, these advantages come at the expense of the impulse charging current issue, hindering the implementation of this topology in practical applications. In addition, nonuniform operation of SC-CMIs is also a challenge that does not fulfill the modularity characteristic of CMI.

II - LITERATURE REVIEW

X. Yuan, **et. al., (**2017) presented four methods to derive multilevel converter topologies.

Many existing topologies as well as new topologies can be derived with the methods presented in this paper. The fundamental characteristics of the multilevel converters which determine their usability such as dc-link neutral point voltage balancing and flying capacitor voltage control are also investigated in this paper with a mathematical model and an example.

K. K. Gupta, et. al., (2016) proposed multilevel inverter topologies with reduced power switch count are reviewed and analysed. The paper will serve as an introduction and an update to these topologies, both in terms of the qualitative and quantitative parameters. Also, it takes into account the challenges which arise when an attempt is made to reduce the device count.

III - SYSTEM IMPLEMENTATION

1. PROPOSED SYSTEM

The proposed system design a novel dual-T-type five-level CMI topology for Photovoltaic panel. It is capable of five levels generation with double voltage boosting gain. This system resolved the impulse current and nonuniform operation problems of SC-CMIs. The inverter switches are controlled with the help of fuzzy logic controller. The fuzzy logic is heuristic controllers which can accurately control the operation of IGBT. The main idea is to integrate a half bridge and an inductor to soft charge a capacitor that is connected in series with the dc source. The capacitor enables the voltage gain boosted to two, while the control of eight power switches that constitutes a dual-T structure enables five voltage levels generation.

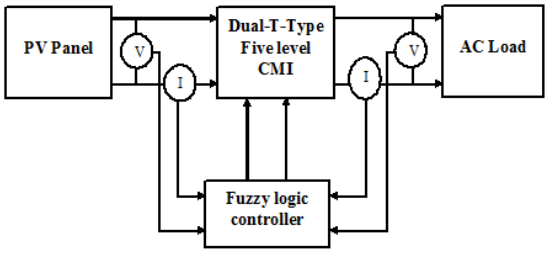


Fig.1 Proposed Block Diagram

2. DUAL-T-TYPE FIVE-LEVEL CASCADED MULTILEVEL INVERTER

The topology of the proposed dual-T-type five-level CMI (DTT-5L-CMI) is depicted in Fig.2 Voltage boosting is achieved by connecting a capacitor C in series with the input dc source. To prevent the impulse charging current as in the case of SC-CMI, an inductor L that is controlled by a half bridge (S5 and S6) is integrated in the topology to achieve soft charging. The rest of the switches constitute two T-type inverters for ac voltage generation.

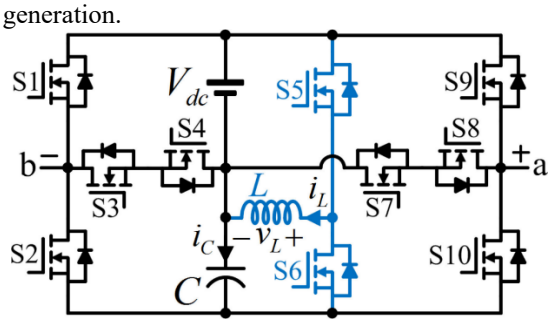
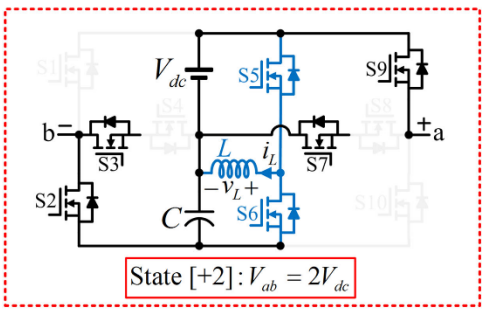


Fig.2 Proposed DTT-5L-CMI

A. Steady-State Analysis

The switching states of the proposed DTT-5L-CMI are analyzed and summarized in Fig.3.With capacitor C charged to Vdc, the maximum voltage level is $2V$dc. Five symmetrical voltage levels are generated in between $2V$dc and $-2V$dc.

Some switches are turned ON despite they are not conducting load current so as to provide a commutation path for the inductive load current during dead time. Taking state [0] as an example, S3 and S8 are two nonconducting switches that are turned ON to cater for the dead-time commutation. Considering the case when there is a voltage level transition from 0 V to Vdc, both S7 and S10 are OFF to prevent short circuit across capacitor C. Assuming an inductive load with S8 is ON, the negative load current can freewheel through S8 as well as the antiparallel diode of S7. The load voltage will eventually clamped to Vdc during dead time, ensuring smooth transition from 0 V to Vdc. On the other hand, if S8 is OFF, the negative load current is forced to flow through the antiparallel diode of S9. A voltage spike of $2V$dc will be generated during dead time, which is highly undesirable. It is therefore important for all the switching states to be design with careful consideration to avoid voltage spike during switch transitions. For achieving soft charging of capacitor C, S5 and S6 are controlled complementary with a constant duty cycle of 0.5. Energy is stored temporarily into inductor L by turning ON S5 before it is discharged to capacitor C when S6 is switched ON. To reduce cost, S6 can be replaced with a diode. However, active power MOSFET is recommended in view of its bidirectional power flow capability.



(a)

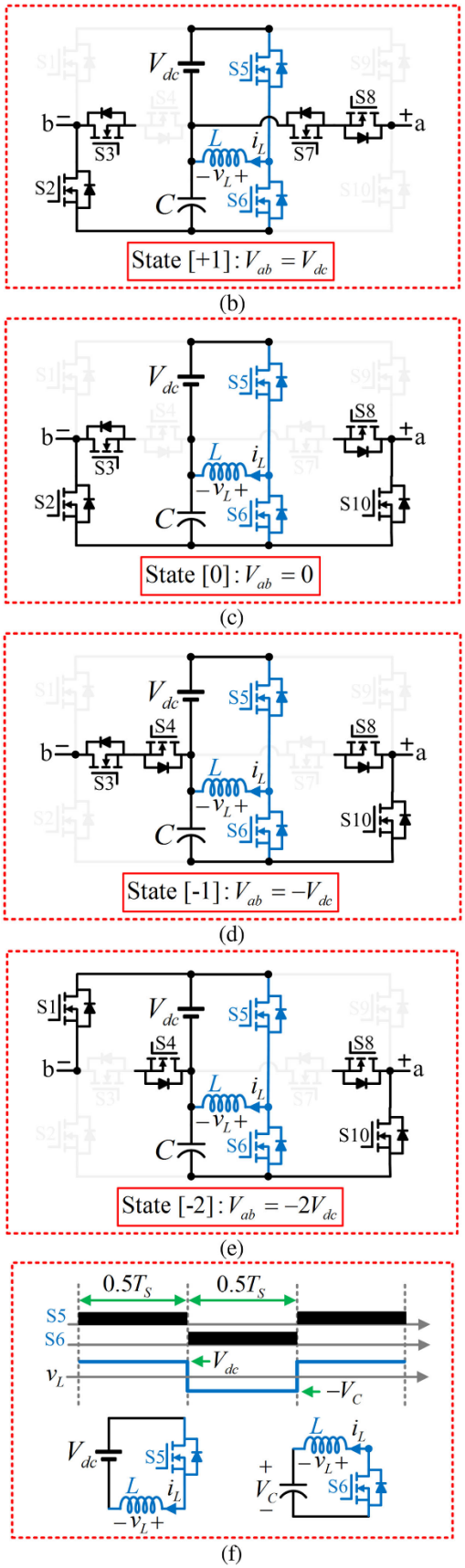


Fig.3 Switching states of the proposed DTT-5L-CMI: (a) state [+2], (b) state [+1], (c) state [0], (d) state [−1], (e) state [−2], and (f) soft charging of *C*

The switching states in Fig.3 shows that switches S1, S2, S5, S6, S9, and S10 each blocks a maximum voltage of 2*V*dc, while voltage stress on the remaining switches are restricted to *V*dc. On the other hand, the current conduction path analyzed in Fig.3 depicts that the current stress on S5 and S6 are determined by the inductor current, while that on the remaining switches are equal to load current.

B. Fuzzy Logic System

A fuzzy logic system (FLS) can be defined as the nonlinear mapping of an input data set to a scalar output data. A FLS consists of four main parts: fuzzifier, rules, inference engine, and defuzzifier. These components and the general architecture of a FLS is shown in Figure.4. The process of fuzzy logic is explained in Algorithm 1: Firstly, a crisp set of input data are gathered and converted to a fuzzy set using fuzzy linguistic variables, fuzzy linguistic terms and membership functions. This step is known as fuzzification. Afterwards, an inference is made based on a set of rules. Lastly, the resulting fuzzy output is mapped to a crisp output using the membership functions, in the defuzzification step. In order to exemplify the usage of a FLS, consider an air conditioner system controlled by a FLS.

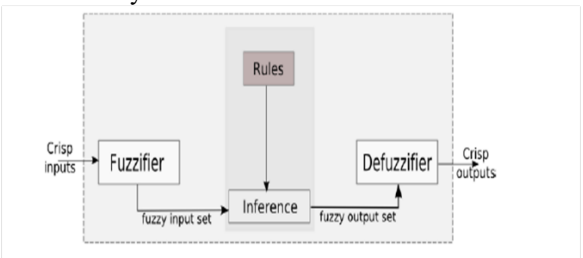


Fig.4 Fuzzy Logic

The process of fuzzy logic is explained in Algorithm 1: Firstly, a crisp set of input data are gathered and converted to a fuzzy set using fuzzy linguistic variables, fuzzy linguistic terms and membership functions. This step is known as fuzzification. Afterwards, an inference is made based on a set of rules. Lastly, the resulting fuzzy output is mapped to a crisp output using the membership functions, in the defuzzification step.

Fuzzy Rules

In a FLS, a rule base is constructed to control the output variable. A fuzzy rule is a simple IF-THEN rule with a condition and a conclusion. In fig.5, sample fuzzy rules for system. It shows the matrix representation of the fuzzy rules for the said FLS. Row captions in the matrix contain the values that current room temperature can take, column captions contain the values for target temperature, and each cell is the resulting command when the input variables take the values in that row and column.

e / de	NL	NM	NS	ZE	PS	PM	PL
NL	NL	NL	NL	NL	NM	NS	ZE
NM	NL	NM	NM	NM	NS	Z	PS
NS	NL	NM	NS	NS	ZE	PS	PM
ZE	NL	NM	NS	ZE	PS	PM	PL
PS	NM	NS	ZE	PS	PS	PM	PL
PM	NS	ZE	PS	PM	PM	PM	PL
PL	ZE	PS	PM	PL	PL	PL	PL
PL	ZE	PS	PM	PL	PL	PL	PL

Fig.5 Fuzzy rules

3. HARDWARE PRESENTATION

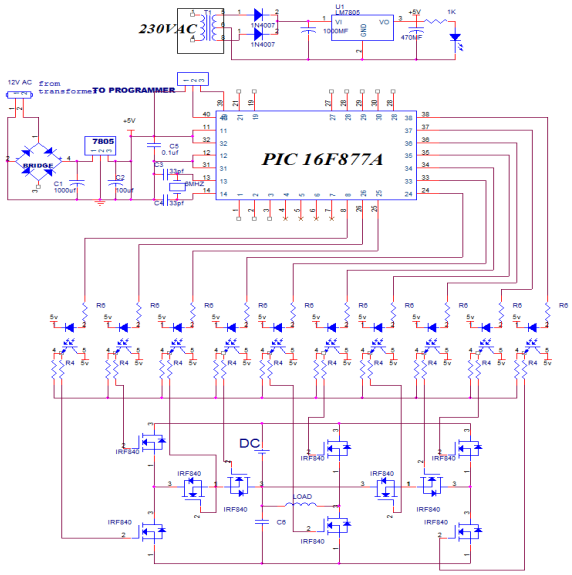


Fig.6 Circuit Diagram

In this fig.6 we are using a five level inverter with MOSFET switches. The output of this circuit is connected to the loads. The each MOSFET are connected with the opto coupler which is connected with the controller ports. The controller we are using are is PIC 16F877A. The switches which are connected at both the primary and secondary side are used for performing the conversion operation and the microcontroller performs the operation as per the user desires. This converter circuit is used for removing the ripples from the source power.

A. PIC16F877A BOARD:

PIC –Peripheral Interface Controller

PIC 16F877 is one of the most advanced microcontroller from Microchip. This controller is widely used for experimental and modern applications because of its low price, wide range of applications, high quality, and ease of availability. It is ideal for applications such as machine control applications, measurement devices, study purpose, and so on.

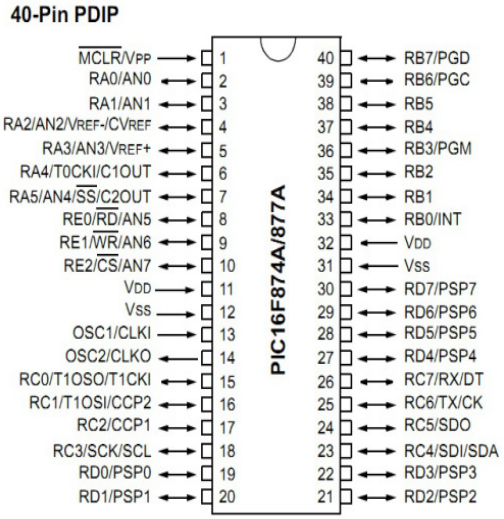


Figure.7 PIC16F877a

B. OPTO COUPLER

In electronics, an **opto-isolator**, also called an **optocoupler**, **photocoupler**, or **optical isolator**, is "an electronic device designed to transfer electrical signals by utilizing light waves to provide coupling with electrical isolation between its input and output". The main purpose of an opto-isolator is "to prevent high voltages or rapidly changing voltages on one side of the circuit from damaging components or distorting transmissions on the other side."

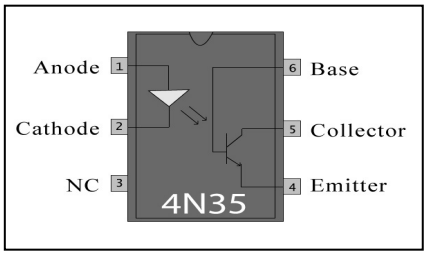


Figure.8 Pin Diagram – 4N35

C. MOSFET

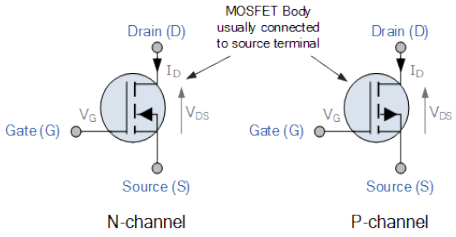


Figure.9 Symbol – IRF840

Third generation Power MOSFETs from Vishay provide the designer with the best combination of

fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC

IV - RESULTS & DISCUSSION

The proposed system model that is designed in MATLAB 2014a Simulink platform. The following figure.10 represents proposed Simulink model.

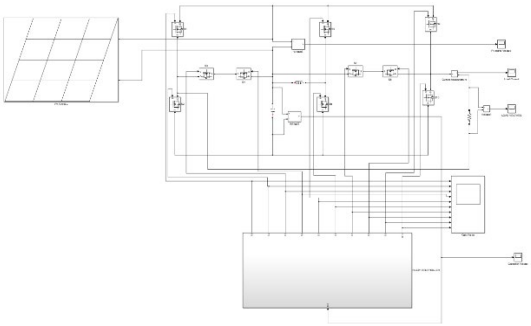


Fig.10 Proposed Simulink model

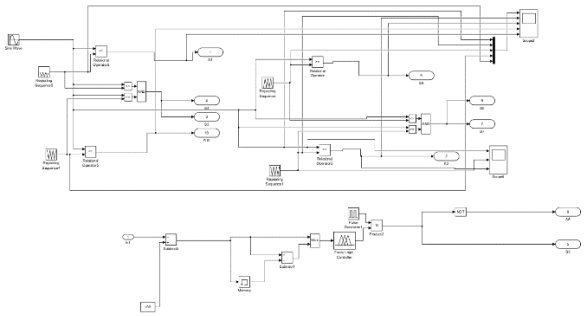


Fig.11 Fuzzy control model

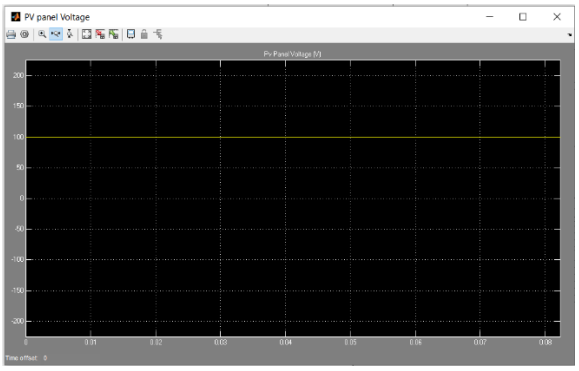


Fig.12 PV panel voltage

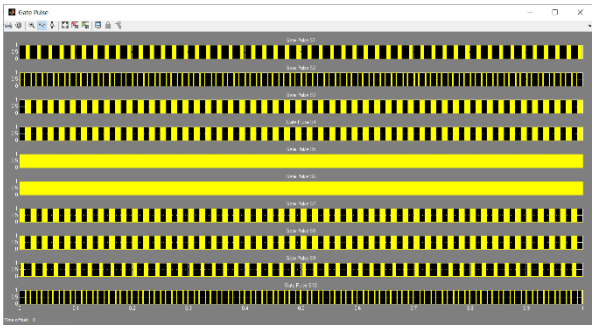


Fig.13 Gate pulse

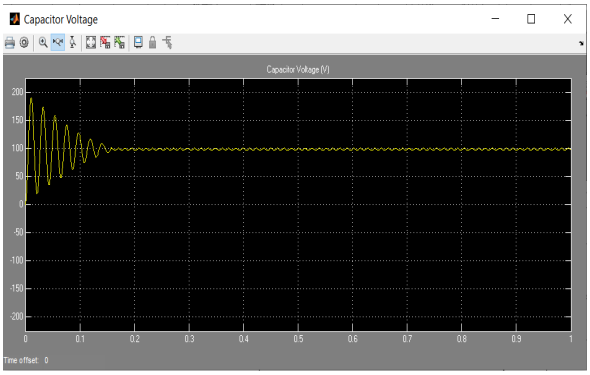


Fig.14 Capacitor voltage

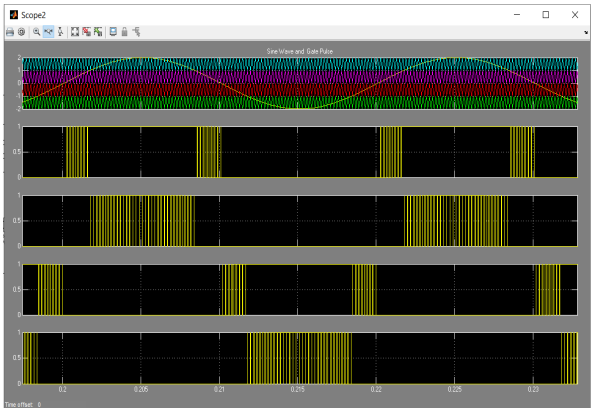


Fig.15 MOSFET pulse

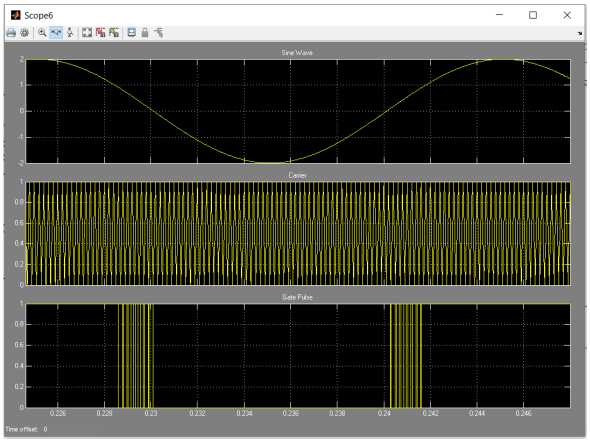


Fig.16 PWM Generation

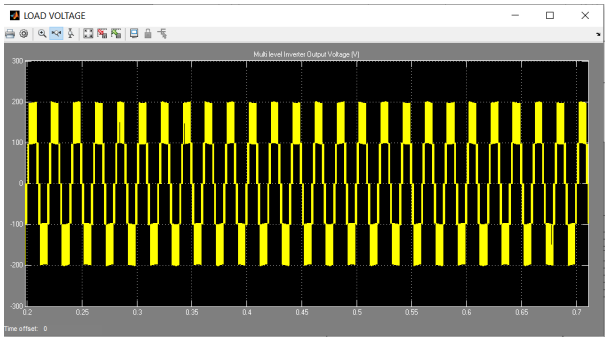


Fig.17 Multilevel inverter output voltage

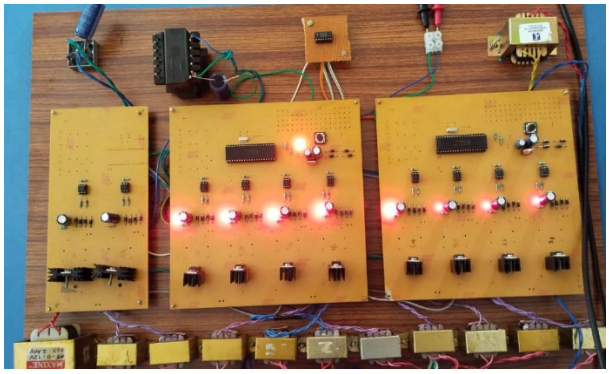


Fig.18 Hardware model

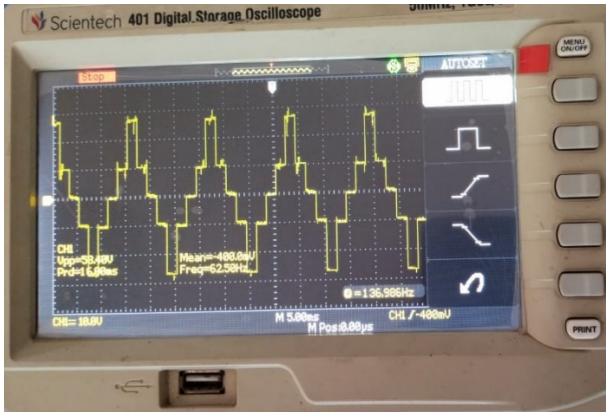


Fig.19 Five level output

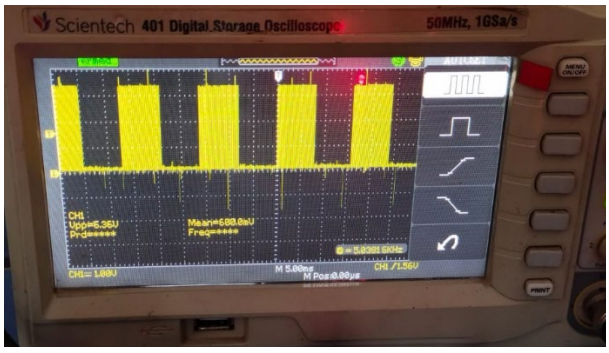


Fig.20 PWM pulse

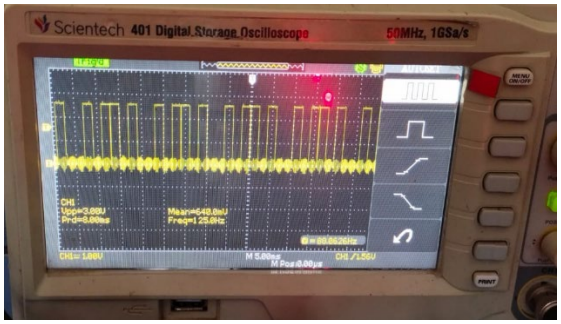


Fig.21 Gate pulse

V - CONCLUSION

In this project, a novel CMI topology is presented by using photovoltaic panel. The proposed DTT-5L-CMI is capable of five levels generation with double voltage boosting gain. The solid state switches are controlled with the help of fuzzy logic controller. Soft charging of capacitor and uniform operation for all cascaded modules are achieved that resolved the problems of recent SC-CMI. Therefore, the proposed topology is an attractive alternative for dc–ac power conversion system.

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