DESIGN OF POWER OPTIMIZED HYBRID ARRAY MULTIPLIER USING SELF TIMED LOGIC

T.Merlin , M.Chitra Evangelin Christina

***Abstract* --- The optimized design of asynchronous array multiplier becomes very complex, which plays a wide role in digital signal processing systems. This paper introduces a high speed hybrid array multiplier with low power consumption. Hybrid array multiplier comprises both single rail and dual rail domino blocks, which resulted the fastest parallel processing and zero gate delay data dependence problem. This proposed array multiplier consumes 56% of power while conventional self timed domino logic consumes 80% in best case analysis. These results are evaluated in 90nm Electronics Design Automation tool simulator.**

***Index Terms*—self timed logic, hybrid full adder, dual rail domino logic, handshaking protocols.**

I. INTRODUCTON

The design of VLSI systems becomes more complex. Along with timing optimization and global clock tree, use of synchronization circuit is exploited. Therefore asynchronous system design plays a vital role in system design [4]. It has some following attractive properties: no clock distribution attained timing optimization, low power consumption and smaller coverage area.

In this pipeline communication between stages are done by different handshaking protocols [9]. Those are: four phase bundled data protocol and four phase dual rail data protocol.

Bundled data protocol serves as single rail logic, which introduce fixed matching delay instead of clock distribution. Delay of functional blocks may varied based on number of fan in, for that reason bundled data resulted encoding overhead. This encoding overhead is reduced by dual rail protocol. Four phase dual rail protocol encode each signal as a pair of wires [6]. Precharge logic is functioned as handshaking protocol. Even though encoding overhead avoided, detection outlay increases with the width of data path increasing. The multilevel pipeline stages consequences larger detection outlay, these will be reduced in proposed pipeline architecture. The proposed structural design hybrid s-logic and dual logic functional blocks, communication between both logics are realized by encoders and precharge/evaluation detectors [10]. This design essentially pondering the design of efficient longest path construction, critical path management attained by way of dual rail logic while remaining paths in s-logic design. Ultimately this proposed design has lower power consumption with reduced bottleneck effect [8]. The reduction of outlays resulted flexible pipeline architecture in complex VLSI system designs. Throughput of this wave pipeline is two times larger than other structural designs with avoiding external storage elements.

In this paper section II illustrates proposed pipeline structural design; section III, IV describes the benefits of suggested pipeline with evaluation results. Section V presents the conclusion.

II. PROPOSED ARCHITECTURE

The structural design of traditional array multiplier has two major blocks: parallel multiplier and sequential full adder. On the other hand the proposed hybrid array multiplier having synchronized multiplier block and xnor based full adder. Where synchronizing logic produce dual rail output with its complementary, while xnor based single bit full adder produce single rail outputs. Therefore these two blocks are operated in different clock domains; hence this architecture is named as hybrid array multiplier. In which the problem of clock distribution is managed by using encoding handshaking protocol between serial synchronizer and parallel xnor adder.

A. Modified Single Bit Adder

The architecture of modified single bit adder is a combination of Complementary Metal Oxide Semiconductor (CMOS) and Transmission Gate Logic (TGL), which proves that it is also a hybrid full adder [11]. The single bit adder consumes large amount of power than any other blocks in array multiplier, it means that this block having wide fan-in [1].

As a result optimized full adder is needed; it is achieved by introducing optimized hybrid full adder and is shown in Fig. 1. This modified adder is a single rail block having 16 transistors while conventional adders requires 26 transistors.

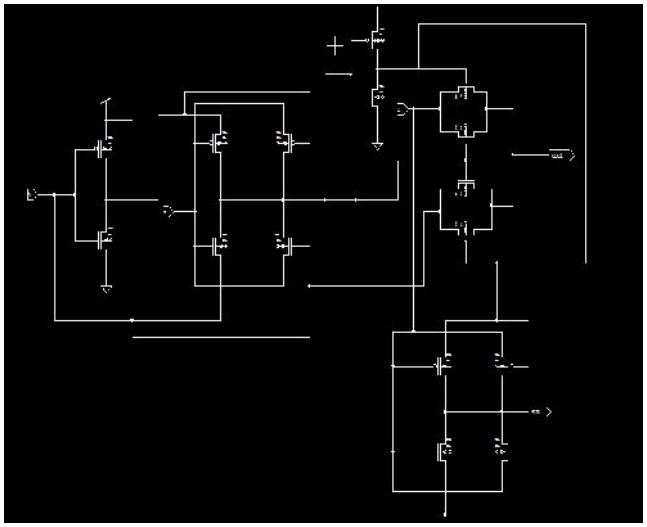

Fig 1. Structural design of modified single bit adder

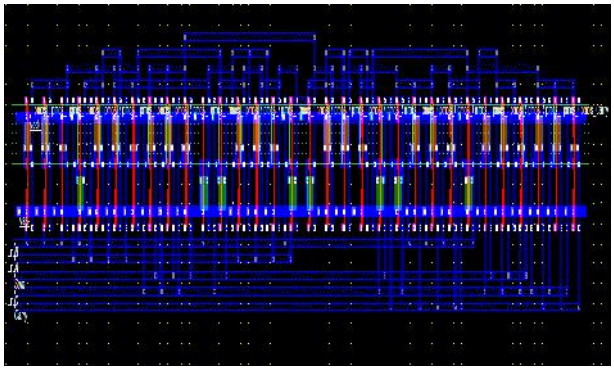

Fig 2. Layout of modified adder

Fig. 2 shows the layout of proposed single bit adder, it consumes the surface area of 275.1µm2 (width786λ, height140λ) whereas conventional adder having 531.2µm2 (width1362λ, height156λ) in 90nm digital circuit design methodology. Although this adder covers 12.7% of area in total layout, traditional single rail adder covering 13.5%.

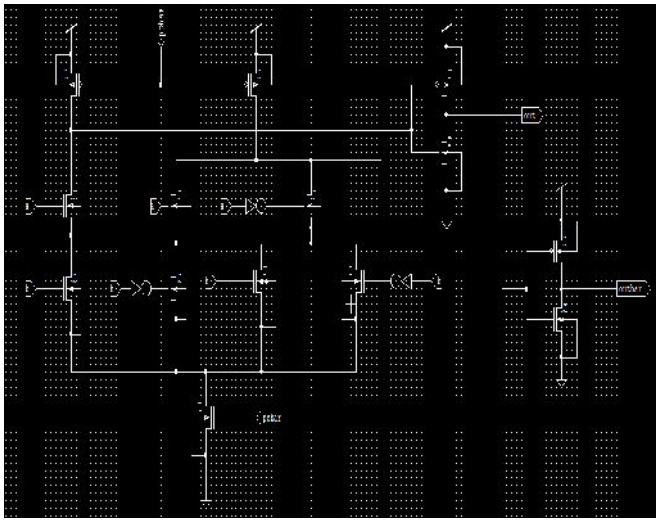

Fig 3. Structural design of synchronized logic gate

B. Parallel Bit Multiplier

Timing specification for multiplication becomes complicated in self timed domino logic design and performing wide role in array multiplier architecture.

The standard CMOS AND gate resulted gate delay- data dependence problem and encoding overhead due to variable number of transistors in every stacks [2]. These problems were avoided by optimized synchronizing parallel multiplier. Fig. 3 proves that all stacks having equal number of transistors, which assures that no data dependence problem and encoding overhead in the performance of array multiplier.

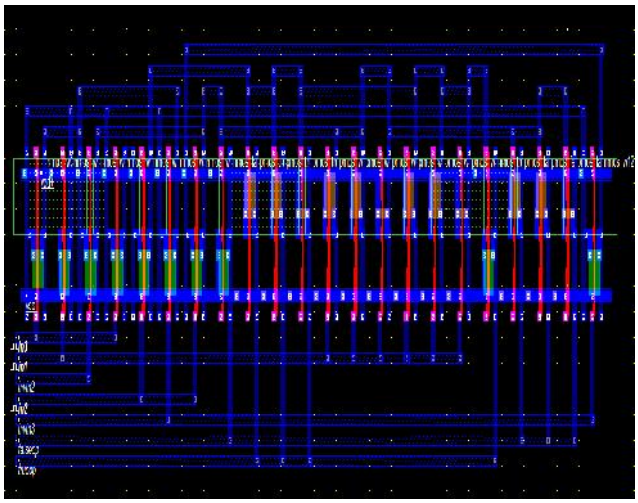

Fig 4. Layout of synchronizing logic gate

Fig. 4 illustrates the layout of proposed synchronizing logic gate, it consumes the surface area of 223.9µm2 (width546λ, height164λ) whereas standard CMOS domino logic having 184.9µm2 (width474λ, height156λ) in 90nm digital circuit design methodology. Although this parallel bit multiplier covers 4.6% of area in total layout, traditional single rail adder covering 5.3%.

C. Synchronizer

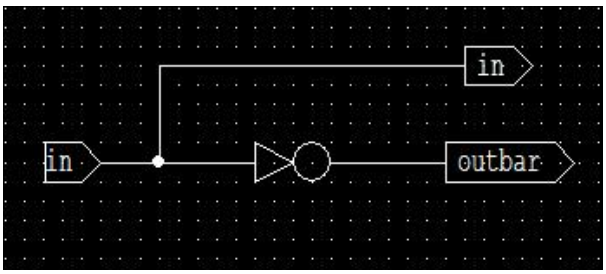

Fig 5. Structural design of synchronizer

In the architecture of array multiplier, modified full adder suggested in single rail logic (SR) at the same time parallel bit multiplier is proposed in dual rail domino logic (DR). Both are operated in different clock domains, which are

coordinated by using synchronizer [3]. It accepts single input from SR logic blocks and produce dual outputs to DR logic blocks.

III. RESULT AND DISCUSSION

This section includes the analysis of proposed planning and experimental results of 4 x 4 array multiplier. Table 1 verified that the suggested hybrid adder requires 43% less components than standard complementary metal oxide semiconductor adder and it covers lower vicinity of 275.1 µm2.

Table 1. Evaluation of projected adder with standard design in 90 nm technology

Performance parameters	Standard full adder	Deliberated Planned hybrid adder
No. of transistors used	28	16
Area (width, height)	53µm2 (68.1µm, 7.8µm)	275.1µm2 (39.9µm, 7.0µm)
Power consumed (at best case analysis)	395.7mw	187.4mw
Speed (GHZ)	3.84	6.67
Latency	1.27ns	910.68ps

The operation speed of proposed adder is 73% faster than conventional design while it consumes 53% less power than standard adder. As a result this designing methodology introduce optimized adder model in self timed logic design.

Table 2. Evaluation of modified AND gate with domino logic style in 90 nm technology

Performance parameters	Conventional domino logic AND	Deliberated synchronizing AND gate
No. of transistors used	11	20
Area (width, height)	184.9µm2 (23.7µm, 7.8µm)	223.9µm2 (27.3µm, 8.2µm)
Power consumed (at best case analysis)	233.72mw	534.3mw
Speed (GHZ)	11.11	7.69
Latency	1.64ns	1.09ns

Table 3. Comparing the performance of 4 x 4 array multiplier among various pipelining with 180 nm design

Design summary	SR logic (without pipeline)	DR logic pipelining	Asynchronous pipelining	Proposed hybrid pipeline
No. of MOSFET used	472	716	628	438
Average power consumption	222.43w	380.83w	537.19w	165.77w
Power at worst case analysis	619mw	850mw	905mw	578mw
Power at best case analysis	61mw	182mw	149mw	12mw
Timing specification	10.51ns	12.06ns	13.11ns	7.07ns
Speed (MHZ)	95.15	82.92	76.28	141.44

From table 2, the deliberated synchronizing design requires 9 more transistors than conventional domino - self timed logic design and it covers vicinity of 223.9 µm2. Although it consumes larger power, the operation speed of proposed design is 69% faster than conventional design.

IV.EXPERIMENTAL SETUP

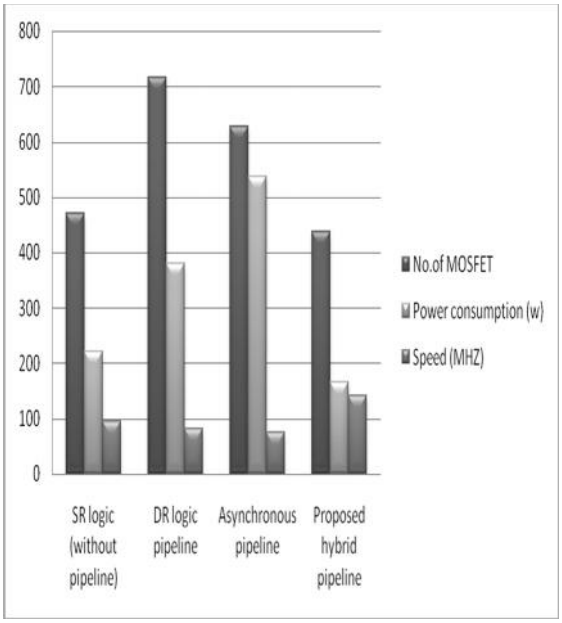

Fig 5. Visual aid for the performance of various pipelines

The tanner 180 nm EDA tool simulator is used to design a 4 x 4 hybrid array multiplier with self timed logic design. This architecture is implemented on a wavepipeline, which has no external storage elements. In that reason the resulted architecture provide high speed 4 x 4 array multiplier in wave pipelining. The suggested methodology has following advantages: consumes ultra low power, produces less forward latency, covering less vicinity and it leads to fastest digital circuit design.

Fig. 5 explains that the proposed design attains better performance in terms of vicinity, power and operating speed than other pipelines.

V. CONCLUSION

This paper introduces ultra low power and high speed hybrid array multiplier design in pipelining using tanner EDA tool simulator. Each blocks in that architecture enhances the performance of the system, which is evaluated by using 90nm digital circuit design methodology. The portioning of blocks, hybrid circuit design and synchronizers results optimized architecture in terms of power, are and forward latency. This system design plays a wide role in digital electronics circuit design and in the systems of digital signal communication in future. The proposed hybrid circuit design offered portable and accurate system designing.

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